

HYBRID MCU/DSP

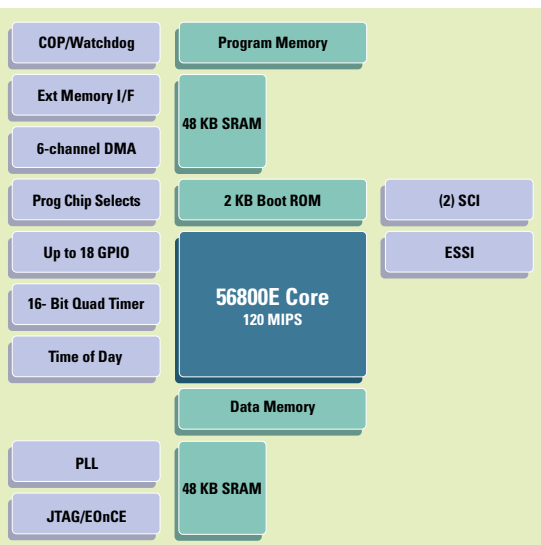
56855

120 MIPS Hybrid Processor

TARGET APPLICATIONS

- Internet audio decoding
- DTAD
- Voice recognition and command
- Embedded modem/data pump
- Voice processing
- General purpose devices
- Automotive hands-free

The 56855 offers 48 KB of on-chip program SRAM and 48 KB data SRAM in a 100-pin LQFP package. The serial peripheral interface (SPI) and the 8-bit host interface have been removed to provide flexibility with fewer features to meet customer price/performance expectations. This device is ideal for systems that require a DSP with greater on-chip memory in a smaller package, but do not require an extensive peripheral set. The 56855 includes a quad timer module with a signal external output.



BENEFITS

- Easy to program with flexible application development tools
- Supports multiple processor connections
- 16-bit quad timer module (with one external pin) that allows capture/compare functionality, and can be cascaded
- Quad timer module can also be used for simple digital-to-analog conversion functionality
- Enhanced synchronous serial interface with enhanced network and audio modes
- Time of Day for applications requiring clock display
- Flexible 6-Channel Direct Memory Access (DMA) allows both internal and external memory transfers with almost no CPU interruption
- External memory expansion up to 2M words program memory or up to 8M words data memory increases capabilities of device for larger algorithms

56855 16-BIT DIGITAL SIGNAL PROCESSORS

- 120 MIPS at 120MHz
- 48 KB Program SRAM
- 48 KB Data SRAM
- 2 KB Boot ROM
- Access up to 4 MB of program memory or up to 16 MB of data memory
- Chip Select Logic for glueless interface to ROM and SRAM
- Six independent channels of DMA
- Enhanced Synchronous Serial Interface (ESSI)
- Two Serial Communication Interfaces (SCI)
- General purpose 16-bit Quad Timer
- JTAG/Enhanced On-Chip Emulation (OnCE™) for unobtrusive, real-time debugging
- Computer Operating Properly (COP)/Watchdog Timer
- Time of Day (TOD)
- 100-pin LQFP package
- Up to 18 GPIO

ENERGY INFORMATION

- Fabricated in high-density CMOS with 3.3V, TTL-compatible digital inputs
- Wait and Stop modes available

PRODUCT DOCUMENTATION

*DSP56800E
Reference Manual*

Detailed description of the 56800E architecture, 16-bit DSP core processor and the instruction set

Order Number: DSP56800ERM/D

*DSP5685x
User's Manual*

Detailed description of memory, peripherals, and interfaces of the 56853, 56854, 56855, 56857, and 56858

Order Number: DSP5685xUM/D

*DSP56855
Technical Data
Sheet*

Electrical and timing specifications, pin descriptions, and package descriptions

Order Number: DSP56855/D

*DSP56855
Product Brief*

Summary description and block diagram of the core, memory, peripherals and interfaces

Order Number: DSP56855PB/D

**AWARD-WINNING
DEVELOPMENT ENVIRONMENT**

- Processor Expert™ (PE) technology provides a rapid application design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.
- The CodeWarrior™ Integrated Development Environment (IDE) is a sophisticated tool for code navigation, compiling and debugging. A comprehensive set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE, the CodeWarrior tool suite and EVMs create a comprehensive, scalable tools solution for easy, fast and efficient development.

56800E CORE FEATURES

The 56800E core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact code for both DSP and MCU applications. The instruction set is also highly efficient for C compilers, enabling rapid development of optimized control applications. Features of the 56800E core include:

- Efficient 16-bit hybrid controller engine with dual Harvard architecture
- 120 Million Instructions Per Second (MIPS) at 120MHz core frequency
- Single-cycle 16 x 16-bit parallel Multiplier-Accumulator (MAC)
- Four 36-bit accumulators, including extension bits
- 16-bit bidirectional shifter
- Parallel instruction set with unique addressing modes
- Hardware DO and REP loops
- Three internal address buses and one external address bus
- Four internal data buses and one external data bus
- Instruction set supports both DSP and controller functions
- Four hardware interrupt levels
- Five software interrupt levels
- Controller-style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/Enhanced OnCE debug programming interface

56855 MEMORY FEATURES

- Harvard architecture permits up to three simultaneous accesses to program and data memory
- On-chip Memory
 - 48 KB Program SRAM
 - 48 KB Data SRAM
 - 2 KB Boot ROM
- Off-Chip Memory Expansion (EMI)
 - Access up to 4 MB of program memory or up to 16 MB of data memory (using chip selects)
 - Chip Select Logic for glueless interface to ROM and SRAM

56855 PERIPHERAL CIRCUIT FEATURES

- General Purpose 16-bit Quad Timer with one external pin*
 - Two Serial Communication Interfaces (SCI)*
 - Enhanced Synchronous Serial Interface (ESSI) module*
 - Computer Operating Properly (COP)/Watchdog Timer
 - JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, real-time debugging
 - Six independent channels of DMA
 - Time of Day
 - Up to 18 GPIO
- * Each peripheral I/O can be used alternately as a General Purpose I/O

ORDERING INFORMATION

PART	SUPPLY VOLTAGE	PACKAGE TYPE	PIN COUNT	FREQUENCY (MHz)	ORDER NUMBER
DSP56855	1.8V, 3.3V	Low-Profile Quad Flat Pack (LQFP)	100	120	DSP56855BU120
DSP56855	1.8V, 3.3V	Low-Profile Quad Flat Pack (LQFP)	100	120	SPAK56855BU120



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