

HYBRID FLASH SOLUTION

56F807

16-bit Hybrid Controller

TARGET APPLICATIONS

- Conveyors
- UPS
- Servo drives
- Fuel management systems
- Lifts/elevators/cranes
- Underwater acoustics
- Industrial frequency inverters
- Noise cancellation
- General purpose devices
- Switched-mode power supplies

The 56F807 is a member of the 56800 core-based family of Hybrid Controllers. It combines, on a single chip, the processing power of a DSP and the functionality of a microcontroller with a flexible set of peripherals to create an extremely cost-effective solution. Because of its low cost, configuration flexibility, and compact program code, the 56F807 is well-suited for many applications. The 56800 core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact code for both DSP and MCU applications. The instruction set is also highly efficient for compilers to enable rapid development of optimized control applications.



BENEFITS

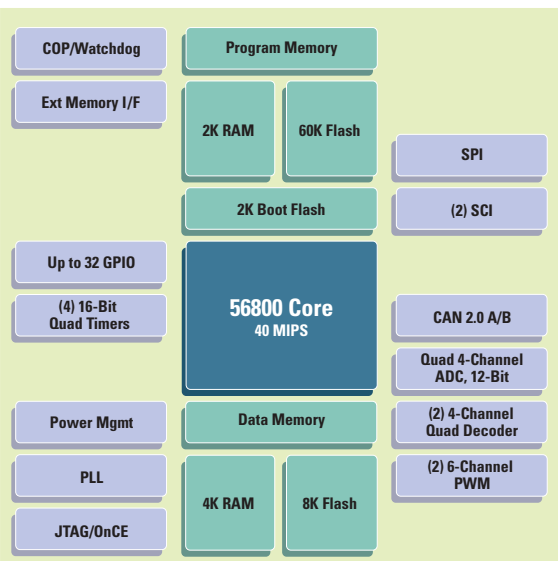
- On-board voltage regulator and power management is designed to reduce overall system cost by allowing for a single supply voltage
- Flash memory is engineered to provide reliable, non-volatile memory storage, eliminating the need for external storage devices
- Easy to program with flexible application development tools
- Simple updating of Flash memory through SPI, SCI or OnCE™, using on-chip boot loader
- Program can boot directly from Flash
- Supports multiple processor connections
- Patented distortion correction in PWM for reducing design risk and better performance control
- PWM and ADC modules are tightly coupled to reduce processing overhead
- Low voltage interrupts protect the system during brownout or power failure
- Simple interface with other asynchronous serial communication devices and off-chip EE memory

56F807 16-BIT HYBRID CONTROLLER

- Up to 40 MIPS at 80MHz core frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- Hardware DO and REP loops
- MCU-friendly instruction set supports both DSP and controller functions: MAC, bit manipulation unit, 14 addressing modes
- 70K On-chip Flash
 - 60K Program Flash
 - 8K Data Flash
 - 2K Boot Flash
- 2K Program RAM
- 4K Data RAM
- Two 6 channel PWM modules
- Four 4 channel, 12-bit ADCs
- Two Quadrature Decoders
- CAN 2.0 A/B module
- Two Serial Communication Interfaces (SCIs)
- Serial Peripheral Interface (SPI)
- Four general purpose Quad Timers
- JTAG/OnCE port for debugging
- 14 dedicated and 18 shared GPIO lines
- 160-pin LQFP or 160 MAPBGA Packages

ENERGY INFORMATION

- Fabricated in high-density CMOS with 5V-tolerant, TTL-compatible digital inputs
- Uses a single 3.3V power supply
- On-chip regulators for digital and analog circuitry to lower cost and reduce noise
- Wait and Stop modes available



HYBRID FLASH SOLUTION

56F807

PRODUCT DOCUMENTATION

DSP56800 Family Manual

Detailed description of the 56800 family architecture, and 16-bit DSP core processor and the instruction set

Order Number: [DSP56800FM/D](#)

DSP56F80x User's Manual

Detailed description of memory, peripherals, and interfaces of the 56F801, 56F802, 56F803, 56F805, and 56F807

Order Number: [DSP56F801-7UM/D](#)

DSP56F807 Technical Data Sheet

Electrical and timing specifications, pin descriptions, and package descriptions

Order Number: [DSP56F807/D](#)

DSP56F807 Product Brief

Summary description and block diagram of the core, memory, peripherals and interfaces

Order Number: [DSP56F807PB/D](#)

AWARD-WINNING DEVELOPMENT ENVIRONMENT

- Processor Expert™ (PE) technology provides a rapid application design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.
- The CodeWarrior™ Integrated Development Environment (IDE) is a sophisticated tool for code navigation, compiling and debugging. A comprehensive set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE, the CodeWarrior tool suite and EVMs create a comprehensive, scalable tools solution for easy, fast and efficient development.

56800 CORE FEATURES

- Efficient 16-bit 56800 family hybrid controller engine with dual Harvard architecture
- As many as 40 Million Instructions Per Second (MIPS) at 80MHz core frequency
- Single-cycle 16 x 16-bit parallel Multiplier-Accumulator (MAC)
- Two 36-bit accumulators including extension bits
- 16-bit bidirectional barrel shifter
- Parallel instruction set with unique addressing modes
- Hardware DO and REP loops
- Three internal address buses and one external address bus
- Four internal data buses and one external data bus
- Instruction set supports both DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/OnCE debug programming interface

56F807 MEMORY FEATURES

- Harvard architecture permits as many as three simultaneous accesses to program and data memory
- On-chip memory including a low-cost, high-volume Flash solution
 - 70K On-chip Flash
 - 60K Program Flash
 - 8K Data Flash
 - 2K Boot Flash
 - 2K Program RAM
 - 4K Data RAM
- Off-chip memory expansion capabilities
 - As much as 64K data memory
 - As much as 64K program memory

56F807 PERIPHERAL CIRCUIT FEATURES

- Two Pulse Width Modulator modules, each with six PWM outputs, three Current Sense inputs, and four Fault inputs, fault-tolerant design with dead-time insertion; supports both center- and edge-aligned modes
- Four 12-bit Analog-to-Digital Converters (ADCs), which support two simultaneous conversions; ADC and PWM modules can be synchronized
- Two Quadrature Decoders
- Four dedicated General Purpose Quad Timers
- Two Serial Communication Interfaces (SCI)
- CAN 2.0 A/B module
- Serial Peripheral Interface (SPI)
- Computer Operating Properly (COP)/ Watchdog timer
- Two dedicated external interrupt pins
- 14 dedicated General Purpose I/O (GPIO) pins, 18 multiplexed GPIO pins
- External reset input pin for hardware reset
- External reset output pin for system reset
- JTAG/OnCE™ for unobtrusive, processor speed-independent debugging
- Software-programmable, Phase Lock Loop-based frequency synthesizer

ORDERING INFORMATION

PART	SUPPLY VOLTAGE	PACKAGE TYPE	PIN COUNT	FREQUENCY (MHz)	ORDER NUMBER
DSP56F807	3.0–3.6V	Low profile Quad Flat Pack (LQFP)	160	80	DSP56F807PY80
DSP56F807	3.0–3.6V	MAP Ball Grid Array (MAPBGA)	160	80	DSP56F807VF80
DSP56F807	3.0–3.6V	Low profile Quad Flat Pack (LQFP)	160	80	SPAK56F807PY80
DSP56F807	3.0–3.6V	MAP Ball Grid Array (MAPBGA)	160	80	SPAK56F807VF80



Motorola and the stylized M Logo are registered in the U.S. Patent and Trademark Office. This product incorporates SuperFlash® technology licensed from SST. All other product or service names are the property of their respective owners. © Motorola, Inc. 2003