WINSTAR Display

OLED SPECIFICATION

Model No:

WEX012864LLPP3N00000

OLED Specification

Contents

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WINSTAR

WINSTAR Display
華凌光電股份有限公司

Technology - Innovation - Value

Eco Friendly - Revolution

WIN YOUR LIFE, STAR YOUR EYES

SPECIFICATION Ver: 0

CUSTOMER :

MODULE NO. : WEX012864LLPP3N00000

APPROVED BY: **(FOR CUSTOMER USE ONLY)**	**PCB VERSION: DATA:**

SALES BY	APPROVED BY	CHECKED BY	PREPARED BY
ISSUED DATE:			

MODLE NO：

RECORDS OF REVISION			DOC. FIRST ISSUE
VERSION	DATE	REVISED PAGE NO.	**SUMMARY**
0	2011.09.22		First issue
A	2011.10.28	7	Correct Operating Temperature

1. Module Classification Information

W E X 012864 L L P P 3 N 00000

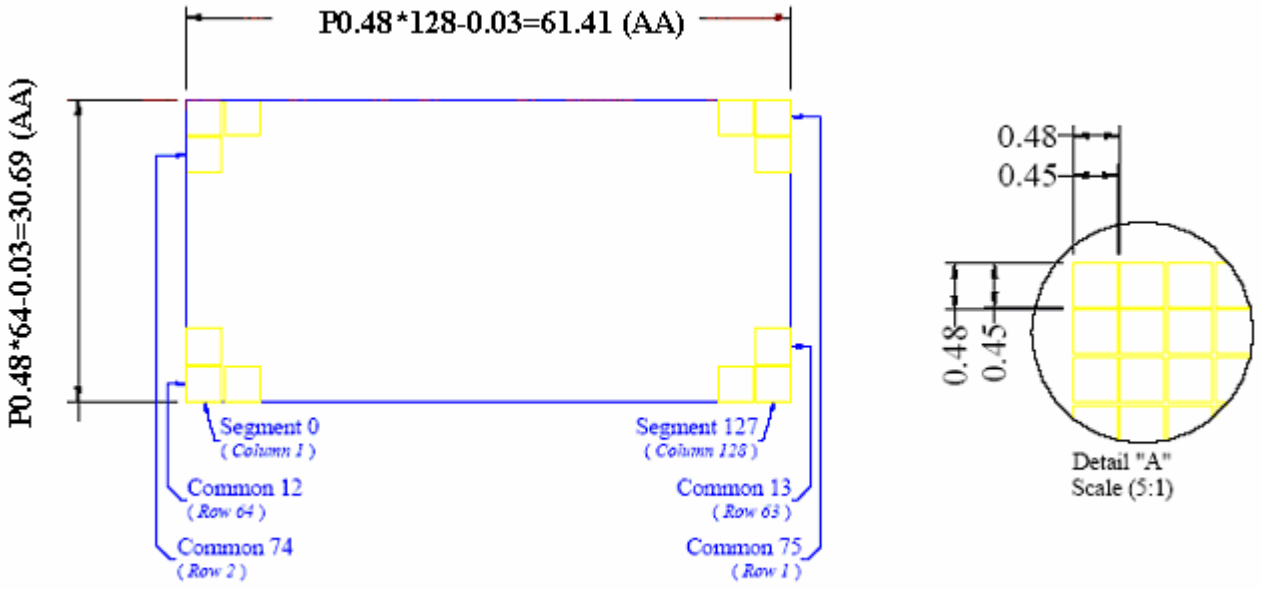
① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨ ⑩ ⑪⑫ ⑬

1	Brand：WINSTAR DISPLAY CORPORATION		
2	E：OLED		
3	Display Type：H→Character Type, G→Graphic Type, X→TAB Type		
4	Number of dots：128 x 64 Dots 8 x2 Dots 16x2 Dots 20x2 Dots 20 x 4 Dots 40x2 Dots 96 x 64 Dots 320X240		
5	Serials code		
6	Emitting Color	A：Amber	R：RED
		B：Blue	C：Full color
		G：Green	W：White
		Y：Yellow Green	L：Yellow
7	Polarizer	P：With Polarizer; N: Without Polarizer	
8	Display Mode	P：Passive Matrix ; A: Action Matrix	
9	Driver Voltage	3: 3.0 V; 5: 5.0V	
10	Touch Panel	N：Without touch panel; T: With touch panel	
11	Products type	0：Standard type 1. Sunlight Readable type 2. Transparent OLED (TOLED) 3. Flexible OLED 4. OLED for Lighting	
12	product grades	product grades: 0：Standard(A-level) 2：B-level 3：C-level 4：high class(AA-level) 5：Customer offerings	
13	Serial No.	Application serial number(00~ZZ)	

2. General Description

Item	Dimension	Unit
Number of Characters	128 Dots x 64 Dots	—
Module dimension	73.0 × 41.86 × 3.4 (mm)	mm
Active Area	61.41 × 30.69 (mm)	mm
Pixel Pitch	0.48 × 0.48 (mm)	mm
Pixel Size	0.45 × 0.45 (mm)	mm
Weight	20.5	g
Display Mode	Passive Matrix	
Display Color	Monochrome (Yellow)	
Drive Duty	1/64 Duty	

Active Area & Pixel Construction



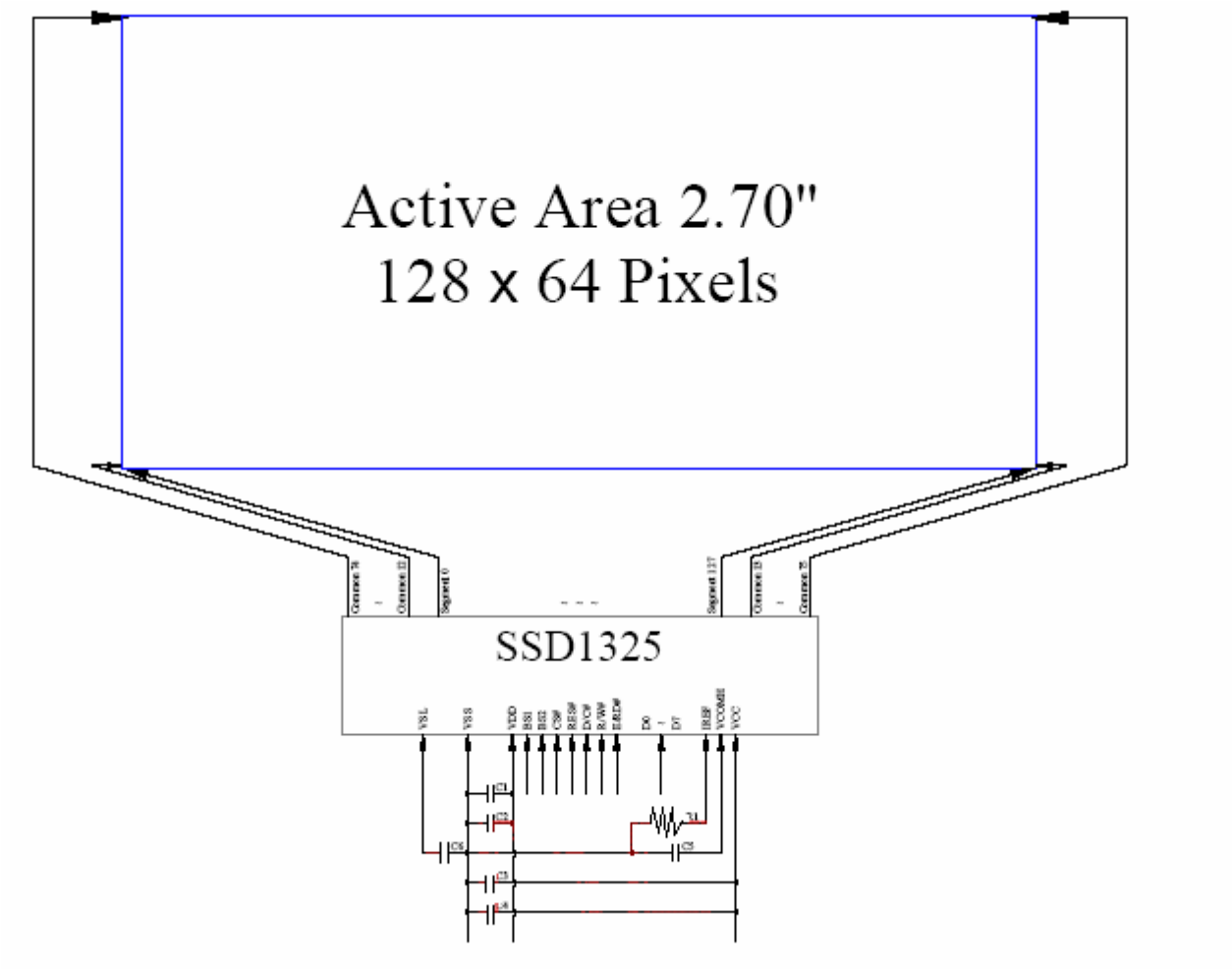
3. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	VDD	-0.3	4	V	1,2
Supply Voltage for Display	VCC	0	16	V	1,2
Operating Temperature	TOP	-40	80	˚C	—
Storage Temperature	TSTG	-40	80	˚C	—

Note 1: All the above voltages are on the basis of “VSS = 0V”.

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 7.“Optics & Electrical Characteristics”. If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

4. Block Diagram



MCU Interface Selection: BS1 and BS2

Pins connected to MCU interface: CS#, RES#, D/C#, R/W#, E/RD#, and D0~D7

C1, C3: 0.1 μ F

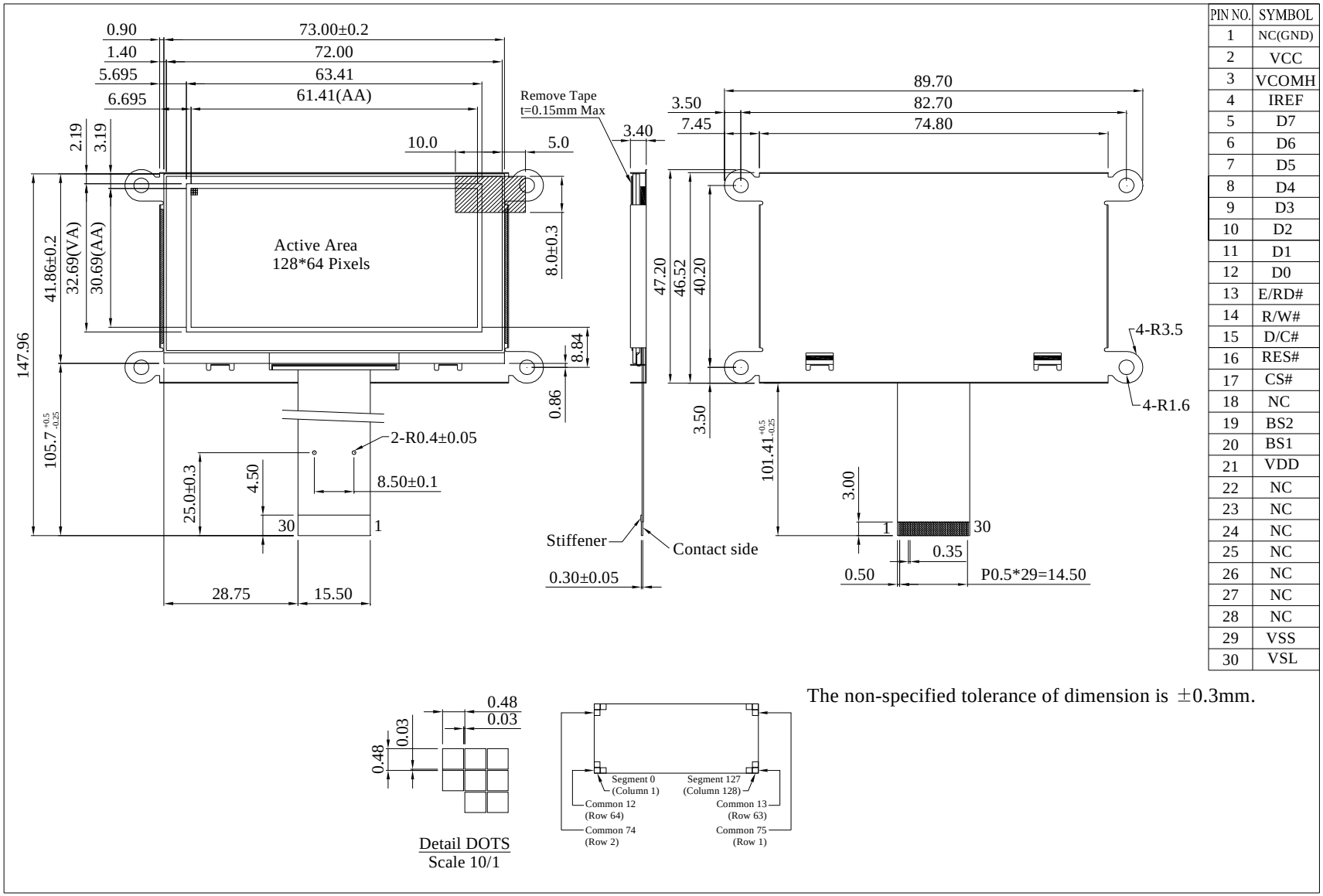
C2, C6: 4.7 μ F

C4: 10 μ F

C5: 4.7 μ F / 25V Tantalum Capacitor

R1: 820kΩ, R1 = (Voltage at IREF - VSS) / IREF

5. Contour Drawing



PIN NO.	SYMBOL
1	NC(GND)
2	VCC
3	VCOMH
4	IREF
5	D7
6	D6
7	D5
8	D4
9	D3
10	D2
11	D1
12	D0
13	E/RD#
14	R/W#
15	D/C#
16	RES#
17	CS#
18	NC
19	BS2
20	BS1
21	VDD
22	NC
23	NC
24	NC
25	NC
26	NC
27	NC
28	NC
29	VSS
30	VSL

The non-specified tolerance of dimension is ±0.3mm.

6. Interface Pin Function

No.	Symbol	I/O	Function
1	NC(GND)		Reserved Pin (Supporting Pin) The supporting pin can reduce the influences from stresses on the function pins. This pin must be connected to external ground.
2	VCC	P	Power Supply for OLED Panel This is the most positive voltage supply pin of the chip. It must be supplied externally.
3	VCOMH	P	Voltage Output High Level for COM Signal This pin is the input pin for the voltage output high level for COM signals. It can be supplied externally or internally. When VCOMH is generated internally, a capacitor should be connected between this pin and VSS.
4	IREF	I	Current Reference for Brightness Adjustment This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 10μA.
5~12	D7~D0	I/O	Host Data Input/Output Bus These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK
13	E/RD#	I	Read/Write Enable or Read This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.
14	R/W#	I	Read/Write Select or Write This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.
15	D/C#	I	Data/Command Control This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the

<table>
<tr><td></td><td></td><td></td><td>Timing Characteristics Diagrams.
When the pin is pulled high and serial interface mode is selected, the data at SDIN is treated as data. When it is pulled low, the data at SDIN will be transferred to the command register.</td></tr>
<tr><td>16</td><td>RES#</td><td>I</td><td>Power Reset for Controller and Driver
This pin is reset signal input. When the pin is low, initialization of the chip is executed.</td></tr>
<tr><td>17</td><td>CS#</td><td>I</td><td>Chip Select
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>18</td><td>NC</td><td></td><td>Reserved Pin
The N.C. pins between function pins are reserved for compatible and flexible design.</td></tr>
<tr><td>19</td><td>BS2</td><td rowspan="2">I</td><td rowspan="2">Communicating Protocol Select
These pins are MCU interface selection input. See the following table:
<table><tr><td></td><td>68XX-parallel</td><td>80XX-parallel</td><td>Serial</td></tr><tr><td>BS1</td><td>0</td><td>1</td><td>0</td></tr><tr><td>BS2</td><td>1</td><td>1</td><td>0</td></tr></table></td></tr>
<tr><td>20</td><td>BS1</td></tr>
<tr><td>21</td><td>Vdd</td><td>P</td><td>Power Supply for Logic Circuit
This is a voltage supply pin. It must be connected to external source.</td></tr>
<tr><td>22</td><td>NC</td><td></td><td rowspan="7">Reserved Pin
The N.C. pins between function pins are reserved for compatible and flexible design.</td></tr>
<tr><td>23</td><td>NC</td><td></td></tr>
<tr><td>24</td><td>NC</td><td></td></tr>
<tr><td>25</td><td>NC</td><td></td></tr>
<tr><td>26</td><td>NC</td><td></td></tr>
<tr><td>27</td><td>NC</td><td></td></tr>
<tr><td>28</td><td>NC</td><td></td></tr>
<tr><td>29</td><td>Vss</td><td>P</td><td>Ground of OLED System
This is a ground pin. It also acts as a reference for the logic pins, the OLED driving voltages, and the analog circuits. It must be connected to external ground.</td></tr>
<tr><td>30</td><td>VSL</td><td>0</td><td>Voltage Output Low Level for SEG Signal
This pin is the output pin for the voltage output low level for SEG signals. A capacitor should be connected between this pin and VSS.</td></tr>
</table>

7. Optics & Electrical Characteristics

7.1 Optics Characteristics

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Brightness	Lbr	With Polarizer (Note 3)	70	100	—	cd/m2
C.I.E. (Yellow)	(x) (y)	Without Polarizer	0.44 0.46	0.48 0.50	0.52 0.54	
Dark Room Contrast	CR		—	>2000:1	—	—
View Angle			>160	—	—	

*** Optical measurement taken at V_{DD} = 2.8V, V_{CC} = 15V.**

Software configuration follows Section 4.4 Initialization.

7.2 DC Characteristics

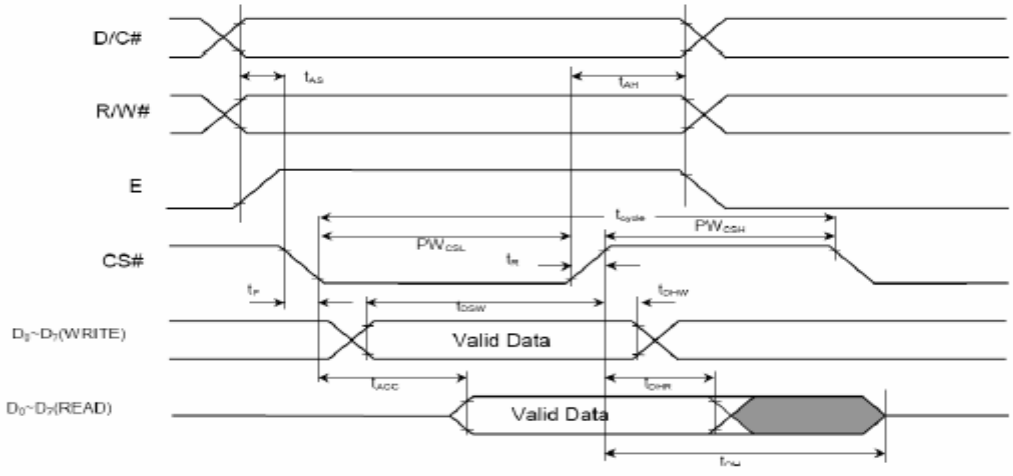
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VCC	Operating Voltage	-	8	12	16	V
VDD	Logic Supply Voltage	-	2.4	2.7	3.5	V
VOH	High Logic Output Level	IOUT = 100uA, 3.3MHz	0.9*VDD	-	VDD	V
VOL	Low Logic Output Level	IOUT = 100uA, 3.3MHz	0	-	0.1*VDD	V
VIH	High Logic Input Level	IOUT = 100uA, 3.3MHz	0.8*VDD	-	VDD	V
VIL	Low Logic Input Level	IOUT = 100uA, 3.3MHz	0	-	0.2*VDD	V
ISLEEP	Sleep mode Current	No loading	-	0.2	5	uA
ICC	**VCC Supply Current** VDD=2.7V, external VCC=12V, IREF=10uA, Frame rate=110Hz, All one pattern, Display on, no loading	Contrast = 7F	-	700	-	uA
IDD	**VDD Supply Current** VDD=2.7V, external VCC=12V, IREF=10uA, Frame rate=110Hz, All one pattern, Display on, no loading	Contrast = 7F	-	-	650	uA
ISEG	**Segment Output Current** VDD=2.7V, VCC=12V, IREF=10uA, Frame rate=110Hz, Display on, Segment pin under test is connected with a 20K resistive load to VSS	Contrast = 7F	270	300	370	uA
		Contrast = 5F	-	225	-	
		Contrast = 3F	-	150	-	
		Contrast = 1F	-	75	-	
Dev	**Segment output current** uniformityVDD=2.7V, VCC=12V, IREF =10uA, Contrast=7F	Adjacent pin	-	±2	-	%
		Overall pin to pin	-	-	±3	
Vcc	DC-DC converter output voltage	VDD input=3V, L=22uH; R1=450Kohm; R2=50Kohm; Icc = 20mA(loading)	10	-	12	V
Pwr	DC-DC converter output power	VDD input=3V, L=22uH; Vcc = 12V	-	-	400	mW

7.3 AC Characteristics

6.3.1 68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	System Cycle Time	300	–	ns
t_{AS}	Address Setup Time	0	–	ns
t_{AH}	Address Hold Time	0	–	ns
t_{DSW}	Write Data Setup Time	40	–	ns
t_{DHW}	Write Data Hold Time	15	–	ns
t_{DHR}	Read Data Hold Time	20	–	ns
t_{OH}	Output Disable Time	–	70	
t_{ACC}	Access Time	–	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read) Chip Select Low Pulse width (Write)	120 60	–	ns
PW_{CSH}	Chip Select High Pulse Width (Read) Chip Select High Pulse Width (Write)	60 60	–	ns
t_R	Rise Time	–	15	ns
t_F	Fall Time	–	15	ns

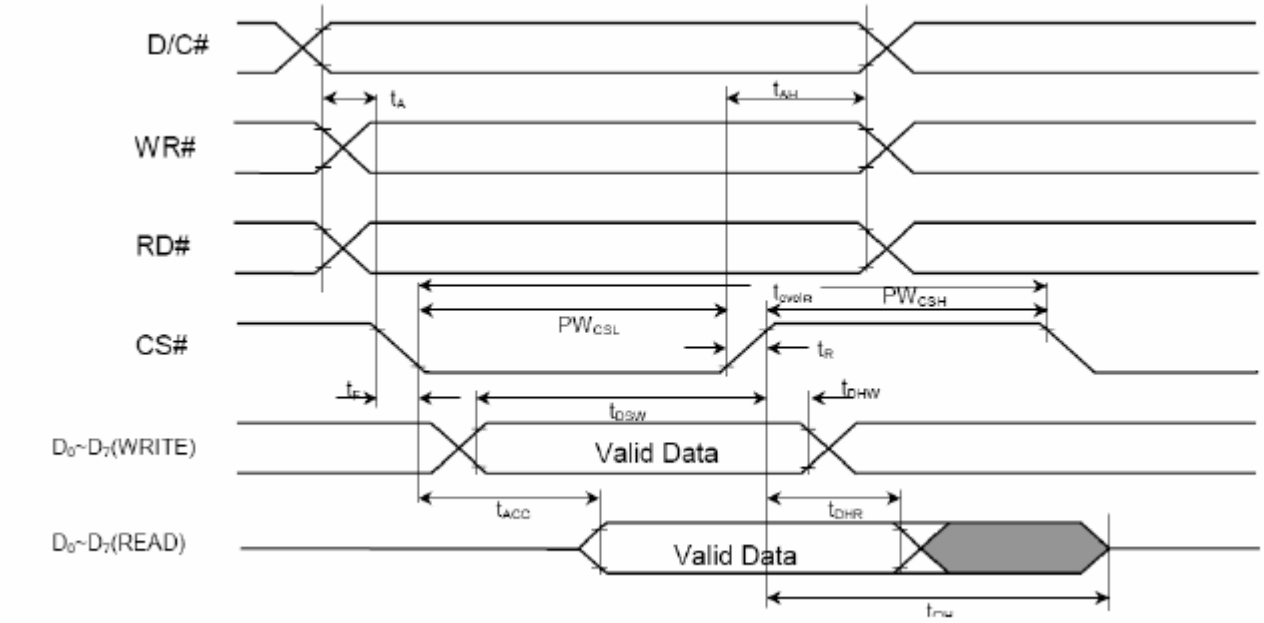
* (V_{DD} - V_{SS} = 2.4V to 3.5V, T_a = 25°C)



7.3.2 80XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	0	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read) Chip Select Low Pulse width (Write)	120 60	-	ns
PW_{CSH}	Chip Select High Pulse Width (Read) Chip Select High Pulse Width (Write)	60 60	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

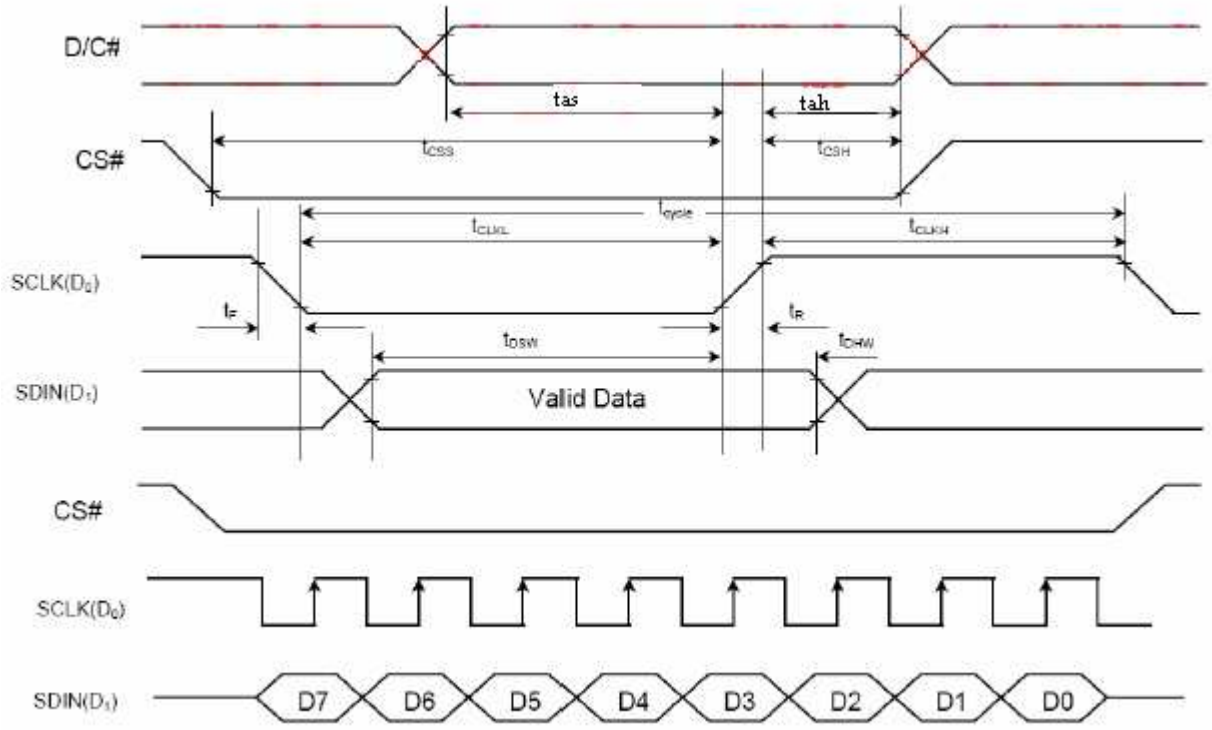
* (V_{DD} - V_{SS} = 2.4V to 3.5V, T_a = 25°C)



7.3.3 Serial Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	250	–	ns
t_{AS}	Address Setup Time	150	–	ns
t_{AH}	Address Hold Time	150	–	ns
t_{CSS}	Chip Select Setup Time	120	–	ns
t_{CSH}	Chip Select Hold Time	60	–	ns
t_{DSW}	Write Data Setup Time	100	–	ns
t_{DHW}	Write Data Hold Time	100	–	ns
t_{CLKL}	Serial Clock Low Time	100	–	ns
t_{CLKH}	Serial Clock High Time	100	–	ns
t_R	Rise Time	–	15	ns
t_F	Fall Time	–	15	ns

* (V_{DD} - V_{SS} = 2.4V to 3.5V, T_a = 25°C)



8. Reliability

8.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation Low Temperature Operation	80℃,240hrs -40℃,240hrs	The operational functions work.
High Temperature Storage Low Temperature Storage	80℃,240hrs -40℃,240hrs	
High Temperature/Humidity Operation/ Thermal Shock	60℃,90%RH,120hrs，-40℃80℃，24cycles 1 hr dwell	

* The samples used for the above tests do not include polarizer.

* No moisture condensation is observed during tests.

8.2 Lifetime

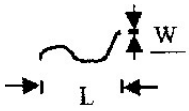
Parameter	Min	Typ	Max	Unit	Condition	Notes
Operating Life Time		100,000	—	Hrs	80 cd/m2, 50% Checkerboard	6

Note 6: The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

8.3 Failure Check Standard

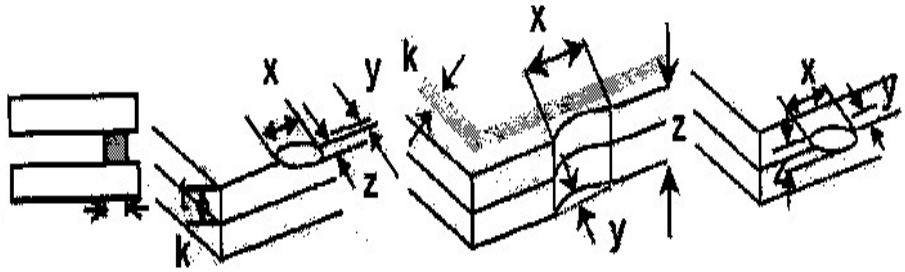
After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5℃; 55±15% RH.

9. Inspection specification

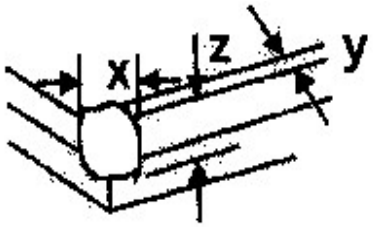
<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>01</td><td>Electrical Testing</td><td>1.1 Missing vertical, horizontal segment, segment contrast defect.
1.2 Missing character , dot or icon.
1.3 Display malfunction.
1.4 No function or no display.
1.5 Current consumption exceeds product specifications.
1.6 Viewing angle defect.
1.7 Mixed product types.
1.8 Contrast defect.</td><td>0.65</td></tr>
<tr><td>02</td><td>Black or white spots (display only)</td><td>2.1 White and black spots on display ≦0.25mm, no more than three white or black spots present.
2.2 Densely spaced: No more than two spots or lines within 3mm</td><td>2.5</td></tr>
<tr><td rowspan="2">03</td><td rowspan="2">Black spots, white spots, contamination (non-display)</td><td>3.1 Round type : As following drawing
Φ=(x + y) / 2</td><td>2.5</td></tr>
<tr><td>3.2 Line type : (As following drawing)
 

<table>
<tr><th>Length</th><th>Width</th><th>Acceptable Q TY</th></tr>
<tr><td>---</td><td>W≦0.02</td><td>Accept no dense</td></tr>
<tr><td>L≦3.0</td><td>0.02＜W≦0.03</td><td rowspan="2">2</td></tr>
<tr><td>L≦2.5</td><td>0.03＜W≦0.05</td></tr>
<tr><td>---</td><td>0.05＜W</td><td>As round type</td></tr>
</table></td><td>2.5</td></tr>
<tr><td>04</td><td>Polarizer bubbles</td><td>If bubbles are visible, judge using black spot specifications, not easy to find, must check in specify direction.
<table>
<tr><th>Size Φ</th><th>Acceptable Q TY</th></tr>
<tr><td>Φ≦0.20</td><td>Accept no dense</td></tr>
<tr><td>0.20＜Φ≦0.50</td><td>3</td></tr>
<tr><td>0.50＜Φ≦1.00</td><td>2</td></tr>
<tr><td>1.00＜Φ</td><td>0</td></tr>
<tr><td>Total Q TY</td><td>3</td></tr>
</table></td><td>2.5</td></tr>
</table>

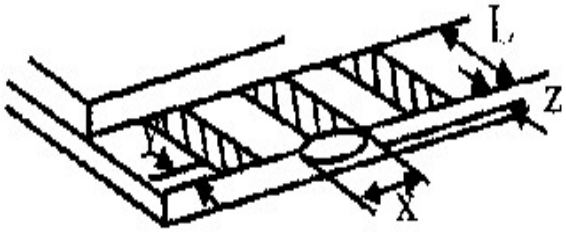
<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>05</td><td>Scratches</td><td>Follow NO.3 Black spots, white spots, contamination</td><td></td></tr>
<tr><td>06</td><td>Chipped glass</td><td>
Symbols Define:
x: Chip length y: Chip width z: Chip thickness
k: Seal width t: Glass thickness a: Side length
L: Electrode pad length:

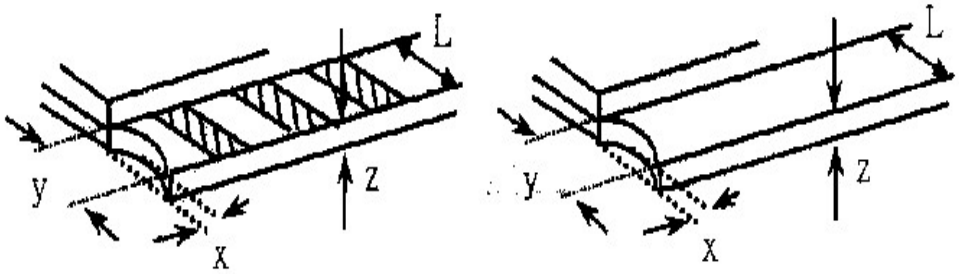
6.1 General glass chip :
6.1.1 Chip on panel surface and crack between panels:


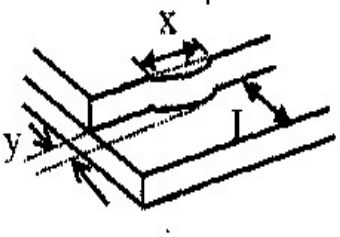
<table>
<tr><th>z: Chip thickness</th><th>y: Chip width</th><th>x: Chip length</th></tr>
<tr><td>Z≦1/2t</td><td>Not over viewing area</td><td>x≦1/8a</td></tr>
<tr><td>1/2t＜z≦2t</td><td>Not exceed 1/3k</td><td>x≦1/8a</td></tr>
</table>
⊙If there are 2 or more chips, x is total length of each chip.

6.1.2 Corner crack:


<table>
<tr><th>z: Chip thickness</th><th>y: Chip width</th><th>x: Chip length</th></tr>
<tr><td>Z≦1/2t</td><td>Not over viewing area</td><td>x≦1/8a</td></tr>
<tr><td>1/2t＜z≦2t</td><td>Not exceed 1/3k</td><td>x≦1/8a</td></tr>
</table>
⊙If there are 2 or more chips, x is the total length of each chip.
</td><td>2.5</td></tr>
</table>

<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>06</td><td>Glass crack</td><td>
Symbols :
x: Chip length y: Chip width z: Chip thickness
k: Seal width t: Glass thickness a: Side length
L: Electrode pad length
6.2 Protrusion over terminal :
6.2.1 Chip on electrode pad :


<table>
<tr><th>y: Chip width</th><th>x: Chip length</th><th>z: Chip thickness</th></tr>
<tr><td>y≦0.5mm</td><td>x≦1/8a</td><td>0 ＜ z ≦ t</td></tr>
</table>
6.2.2 Non-conductive portion:


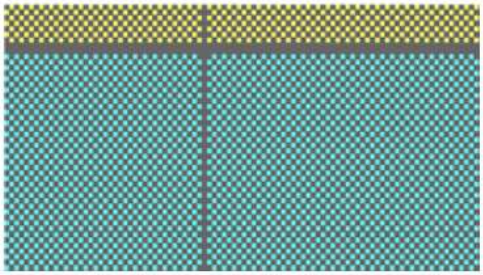
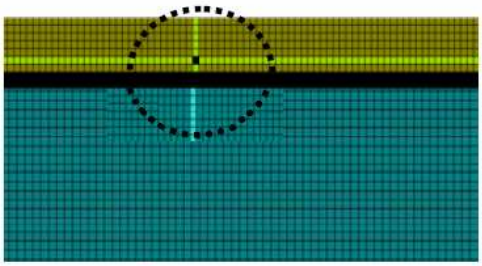
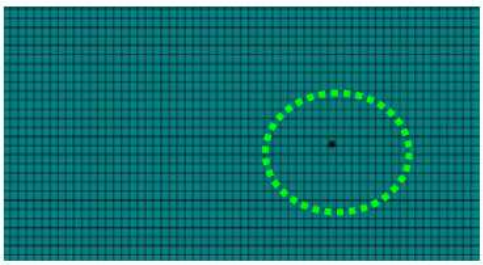
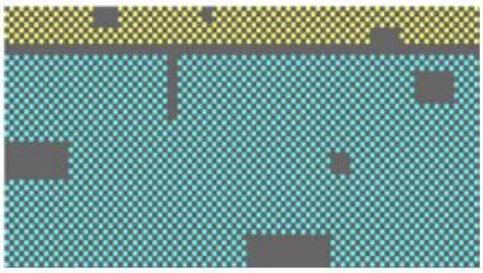
<table>
<tr><th>y: Chip width</th><th>x: Chip length</th><th>z: Chip thickness</th></tr>
<tr><td>y≦ L</td><td>x≦1/8a</td><td>0 ＜ z ≦ t</td></tr>
</table>
⊙If the chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications.
⊙If the product will be heat sealed by the customer, the alignment mark not be damaged.
6.2.3 Substrate protuberance and internal crack.


<table>
<tr><th>y: width</th><th>x: length</th></tr>
<tr><td>y≦1/3L</td><td>x ≦ a</td></tr>
</table>
</td><td>2.5</td></tr>
</table>

NO	Item	Criterion	AQL
07	Cracked glass	With extensive crack is not acceptable.	2.5
08	Backlight elements	8.1 Illumination source flickers when lit. 8.2 Spots or scratched that appear when lit must be judged. Using Spot, lines and contamination standards. 8.3 Backlight doesn't light or color wrong.	0.65 2.5 0.65
09	Bezel	9.1 Bezel may not have rust, be deformed or have fingerprints, stains or other contamination. 9.2 Bezel must comply with job specifications.	2.5 0.65
10	PCB、COB	10.1 COB seal may not have pinholes larger than 0.2mm or contamination. 10.2 COB seal surface may not have pinholes through to the IC. 10.3 The height of the COB should not exceed the height indicated in the assembly diagram. 10.4 There may not be more than 2mm of sealant outside the seal area on the PCB. And there should be no more than three places. 10.5 No oxidation or contamination PCB terminals. 10.6 Parts on PCB must be the same as on the production characteristic chart. There should be no wrong parts, missing parts or excess parts. 10.7 The jumper on the PCB should conform to the product characteristic chart. 10.8 If solder gets on bezel tab pads, LED pad, zebra pad or screw hold pad, make sure it is smoothed down.	2.5 2.5 0.65 2.5 2.5 0.65 0.65 2.5
11	Soldering	11.1 No un-melted solder paste may be present on the PCB. 11.2 No cold solder joints, missing solder connections, oxidation or icicle. 11.3 No residue or solder balls on PCB. 11.4 No short circuits in components on PCB.	2.5 2.5 2.5 0.65

NO	Item	Criterion	AQL
12	General appearance	12.1 No oxidation, contamination, curves or, bends on interface Pin (OLB) of TCP. 12.2 No cracks on interface pin (OLB) of TCP. 12.3 No contamination, solder residue or solder balls on product. 12.4 The IC on the TCP may not be damaged, circuits. 12.5 The uppermost edge of the protective strip on the interface pin must be present or look as if it cause the interface pin to sever. 12.6 The residual rosin or tin oil of soldering (component or chip component) is not burned into brown or black color. 12.7 Sealant on top of the ITO circuit has not hardened. 12.8 Pin type must match type in specification sheet. 12.9 Pin loose or missing pins. 12.10 Product packaging must the same as specified on packaging specification sheet. 12.11 Product dimension and structure must conform to product specification sheet.	2.5 0.65 2.5 2.5 2.5 2.5 2.5 0.65 0.65 0.65 0.65

Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major