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SPECIFICATION

CUSTOMER ： _____

MODULE NO.: WF102ATIFGDAT0#

APPROVED BY: **(FOR CUSTOMER USE ONLY)**	**PCB VERSION:** **DATA:**

SALES BY	APPROVED BY	CHECKED BY	PREPARED BY

VERSION	DATE	REVISED PAGE NO.	SUMMARY
0	2013.02.25		First issue

RECORDS OF REVISION

DOC. FIRST ISSUE

VERSION	DATE	REVISED PAGE NO.	**SUMMARY**
0	2013.02.25		First issue

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1.Module Classification Information

W	F	102	A	T	I	F	G	D	A	T	0	#
①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩	⑪	⑫	⑬

① Brand：WINSTAR DISPLAY CORPORATION
② Display Type：H→Character Type, G→Graphic Type F→TFT Type
③ Display Size：10.2” TFT
④ Model serials no.
⑤ Backlight Type： F→CCFL, White T→LED, White
S→LED, High Light White

⑥ LCD Polarize Type/ Temperature range/ Gray Scale Inversion Direction
I→Transmissive, W. T, 6:00
L→Transmissive, W.T,12:00

⑦ A：TFT LCD
B：TFT+FR+CONTROL BOARD
C：TFT+FR+A/D BOARD
D：TFT+FR+A/D BOARD+CONTROL BOARD
E：TFT+FR+POWER BOARD
F：TFT+CONTROL BOARD
G：TFT+FR
H：TFT+D/V BOARD
I：TFT+FR+D/V BOARD
J：TFT+POWER BD

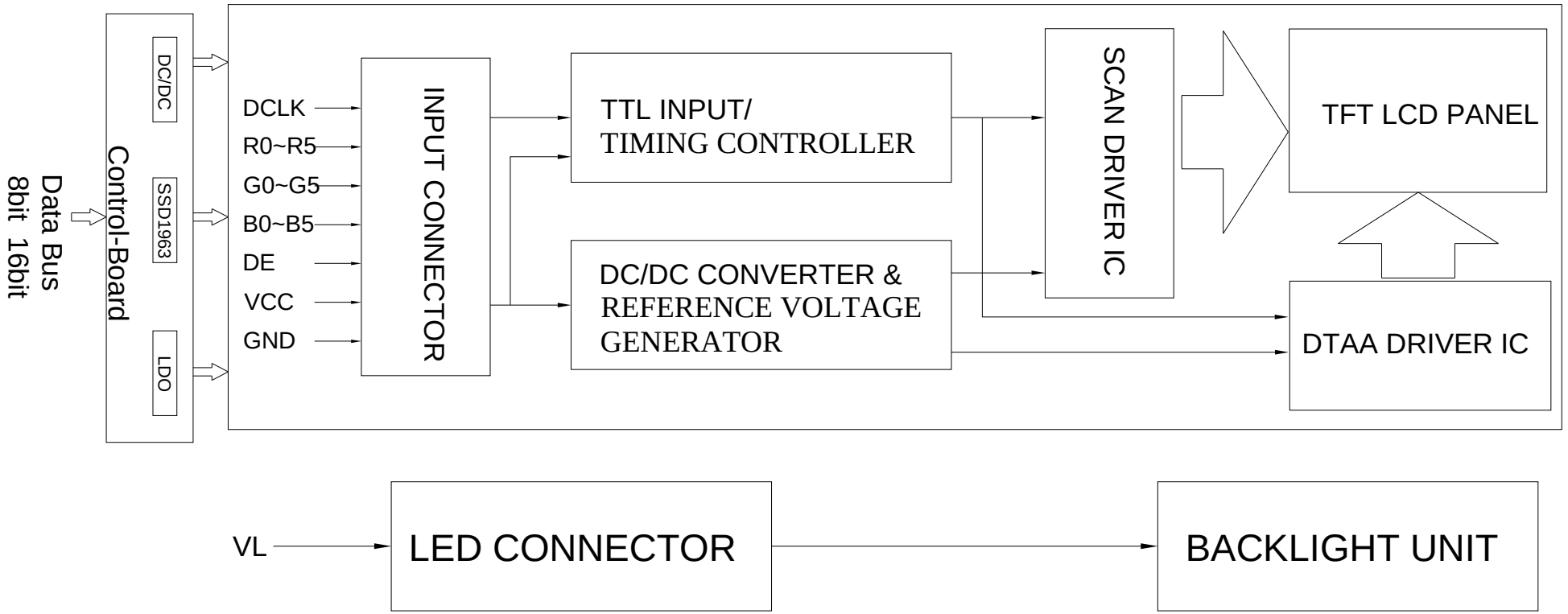
⑧ Solution:
A: 128160 B:320234 C:320240 D:480234 E:480272 F: 640480 G: 800480
⑨ H:1024600 I:320480 J:240320 K:800600 L:240400 M :1024768
⑩ D: Digital L：LVDS
Interface： N：without control board A：8Bit B：16Bit

⑪ TS： N：Without TS T：resistive touch panel C：capacitive touch panel
⑫ Version
⑬ Special Code #:Fit in with ROHS directive regulations

2.General Specification

Parameter		Specifications	Unit
LCD size		10.2(Diagonal)	Inch
Display mode		Normally white, Transmissive type	
Number of Pixel		800 RGB x 480	Dot
Active area		222.0(W) × 132.48(H)	mm
Pixel Pitch		0.0925(W) × 0.276(H)	mm
Pixel Configuration		RGB-Stripe	
Interface		Digital	
Contrast Ratio		300	
View Angle L/R/U/D (CR>10)		65,65,45,65	Degree
View Direction		12 o'clock	
Gray Scale Inversion Direction		6 o'clock	
Outline Dimension		235.0 (H) x145.0 (V) x 8.35 (D)	mm
Weight		350 (typical)	g
Temperature Range	Operation	-20~70	^{0}C
	Storage	-30~80	^{0}C

3.Block Diagram



4.Electrical Characteristics

4-1. ELECTRICAL CHARACTERISTICS OF LCM

ITEM	SYMBOL	CONDITION	MIN.	TYPICAL	MAX.	UNIT
Digital Power Supply Voltages	V_{DD}	V_{DD} -DGND	3.0	3.3	3.6	V
Digital Supply Current Consumption	I_{VDD}	V_{DD}=3.3V	900	1150	1200	mA
Analog Power Supply Voltage	AVDD		8.8	9.0	9.2	V
Analog Supply Current Consumption	IAVDD		-	25	50	mA
Gate Driver Positive Supply Voltage	VGH		15.3	16	16.7	V
Gate Driver Positive Supply Current	IVGH		-	0.3	0.5	mA
Gate Driver Negative Supply Voltage	VGL		-7.7	-7	-6.3	V
Gate Driver Negative Supply Current	IVGL		-	0.2	1.0	mA
Common Electrode Driving Voltage	VCOM	Black Pattern	3.65	3.85	4.5	V
Supply Current for LED B/L	I_{LED}		180	200	220	mA
Supply Voltage for LED B/L	V_{LED}		8.4	9.3	10.5	V
Input Logic Signal High Threshold	VIH		0.7 V_{DD}	-	V_{DD}	V
Input Logic Signal Low Threshold	VIL		0	-	0.3 V_{DD}	V
Brightness	L	White Pattern	-	350	-	cd/m2

＊ Recommended TFT Driving for 25℃

4-2. Gamma Voltage Level

ITEM	SYMBOL	CONDITION	MIN.	TYPICAL	MAX.	UNIT
Gamma Voltage level1~14	V1	AVDD=9V	-	8.875	-	V
	V2		-	8.82	-	V
	V3		-	7.28	-	V
	V4		-	6.725	-	V
	V5		-	6.324	-	V
	V6		-	5.674	-	V
	V7		-	5.181	-	V
	V8		-	3.896	-	V
	V9		-	3.314	-	V
	V10		-	2.665	-	V
	V11		-	2.262	-	V
	V12		-	1.709	-	V
	V13		-	0.17	-	V
	V14		-	0.116	-	V

5.Absolute Maximum Ratings

Item	Symbol	Values		Unit	Remark
		Min	Max		
Power voltage	VCC	-0.3	5	V	
	AVDD	-0.5	12	V	
	VGH	13	19	V	
	VGL	-12	-2	V	
	VGH-VGL	-	31	V	
Input signal voltage	V1~V7	-0.4AVDD	AV_{DD}-0.1	V	Note 1
	V8~V14	-0.3	$0.6AV_{DD}$	V	
Operation temperature	TOP	-20	70	°C	
Storage temperature	TST	-30	85	°C	
LED Reverse Voltage	VR	-	1.2	V	Each LED Note 3
LED Forward Current	IF	-	25	MA	Each LED

Note 1: AV_{DD} - 0.1≧V1≧V2≧V3≧V4≧V5≧V6≧V7≧V8≧V9≧V10>V11≧V12≧V13≧V14≧AVSS + 0.1

Note 2: The absolute maximum rating values of the module should not be exceeded. Once exceeded absolute maximum rating values, the characteristics of the module may not be recovered. Even in an extreme condition, may result in module permanently destroyed.

Note 3: Vr conditions: Zener Diode 20mA.

6.Interface Pin Function

LCM PIN Definition

P/N	Symbol	8 B IT Function
1	GND	Ground
2	VDD	Power supply for Logic
3	NC	No connection
4	RS	Command/Data select
5	WR	8080 family MPU interface : Write signal
6	RD	8080 family MPU interface: Read signal
7	DB0	Data bus
8	DB1	
9	DB2	
10	DB3	
11	DB4	
12	DB5	
13	DB6	
14	DB7	
15	CS	Chip select
16	RES	Reset
17	NC	No connection
18	NC	No connection
19	NC	No connection
20	NC	No connection

LED BACKLIGHT (J1): JST BHSR-02VS-1

Pin No.	Symbol
1	A
2	K

CORRESPONDABLE BACKLIGHT CONNECTOR : SM 02B-BHSS-1

7.Electro-optical Characteristics

Item		Symbol	Condition	Min	Typ	Max	Unit	Note
Response time		TON	θ=0°	-	15	30	ms	Note 3
		TOFF		-	20	40	ms	
Contrast ratio		CR		250	300	-	-	Note 4
Color Chromaticity	White	Wx		0.26	0.31	0.36	%	Note 2,5,6
		Wy		0.28	0.33	0.38		
Viewing Angle	Hor.	θ R	θ=180°	55	65	-	Degree	Note 1
		θ L	θ=0°	55	65	-		
	Ver.	θ T	θ=90°	35	45	-		
		θ B	θ=2700°	55	65	-		
Luminance		L	θ=0°	280	350	-	cd/m2	Note 6
Luminance uniformity		YU	θ=0°	70	75		%	Note 7

Test Conditions:

1. VCC=3.3V, IL=200mA (Backlight current), the ambient temperature is 25℃.
2. The test systems refer to Note 2.

Note 1: Definition of viewing angle range

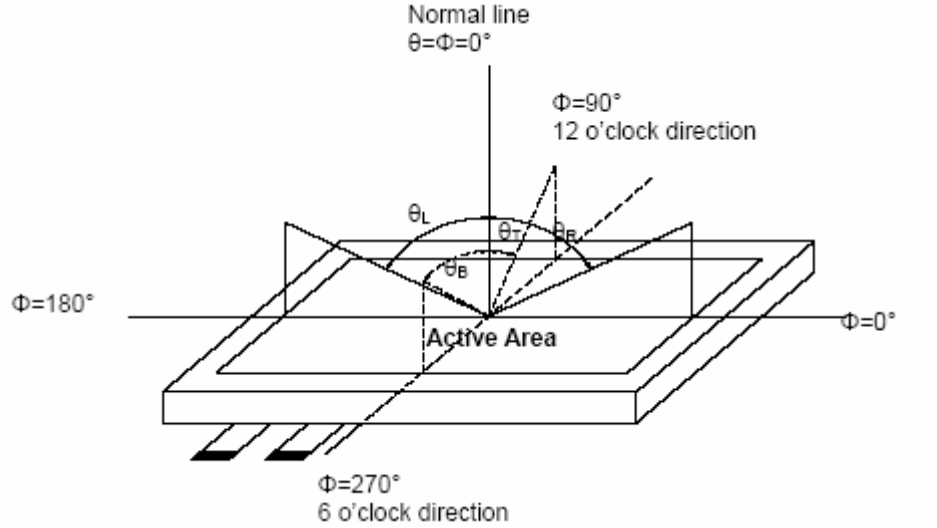


Fig. 4-1 Definition of viewing angle

Note 2: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 30 minutes operation, the optical properties are measured at the center point of the LCD screen. (Response time is measured by Photo detector TOPCON BM-7, other items are measured by BM-5A/Field of view: 1° /Height: 500mm.)

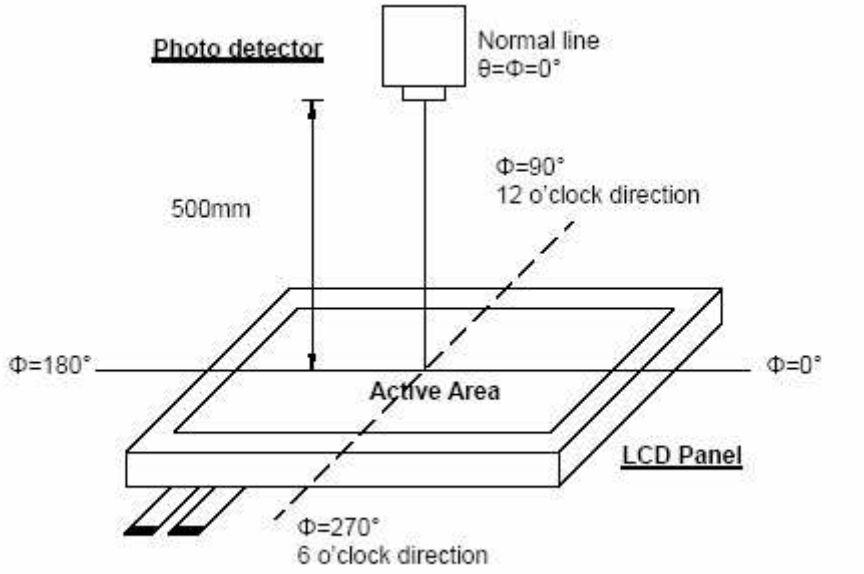


Fig. 4-2 Optical measurement system setup

Note 3: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.

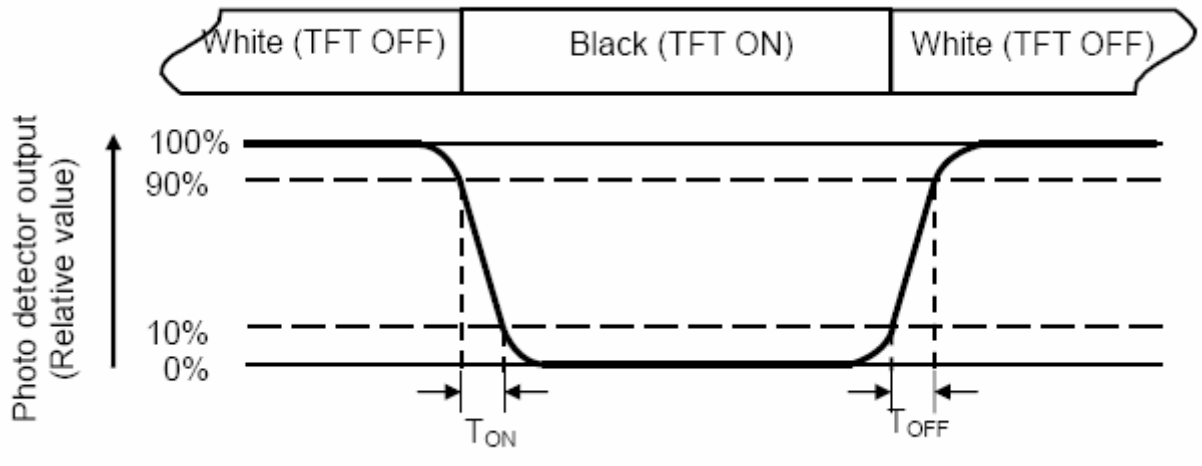


Fig. 4-3 Definition of response time

Note 4: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6: All input terminals LCD panel must be ground when measuring the center area of the panel. The LED driving condition is I_L=200mA.

Note 7: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer to Fig. 4-4).Every measuring point is placed at the center of each measuring area.

$$\textit{Luminance Uniformity (Yu)} = \frac{B_{min}}{B_{max}}$$

L-------Active area length W----- Active area width

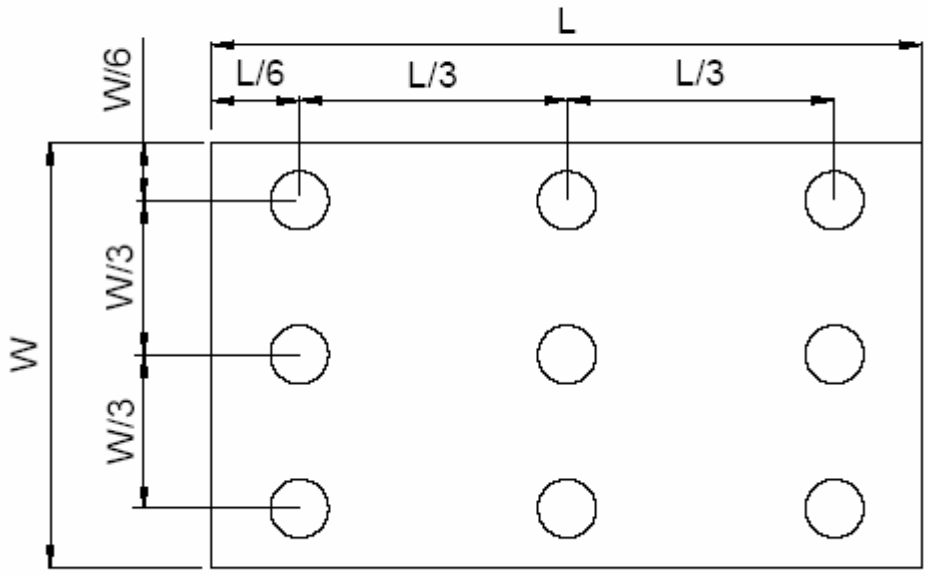
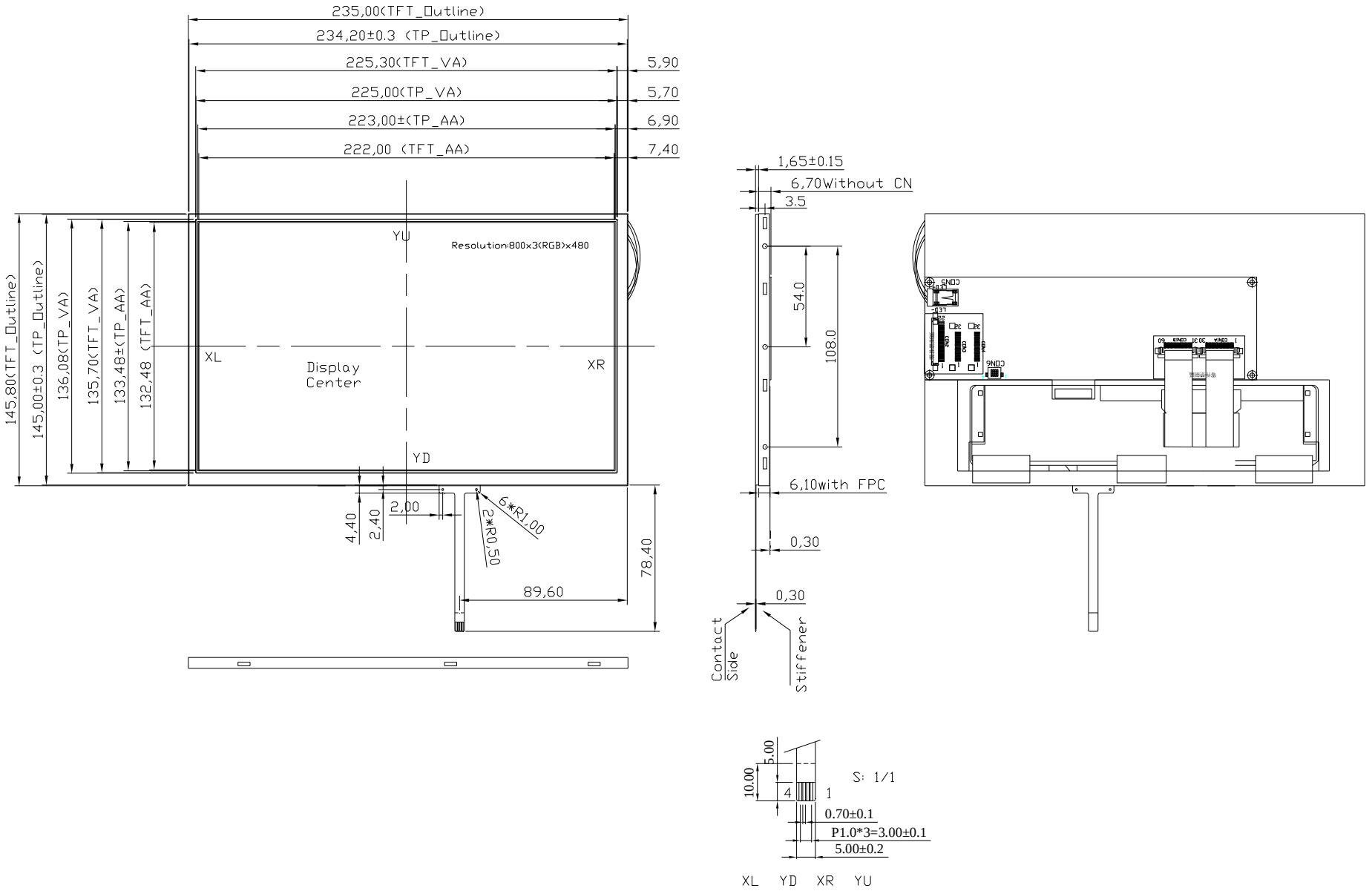


Fig. 4-4 Definition of measuring points

B_{max}: The measured maximum luminance of all measurement position.

B_{min}: The measured minimum luminance of all measurement position.

8. Contour Drawing



9. AC Characteristics

Conditions:

Voltage referenced to VSS

VDDD, VDDPLL = 1.2V

VDDIO, VDDLCD = 3.3V

TA = 25°C

CL = 50pF (Bus/CPU Interface)

CL = 0pF (LCD Panel Interface)

9.1 Clock Timing

Table 9-1:Clock Input Requirements for CLK (PLL-bypass)

Symbol	Parameter	Min	Max	Units
FCLK	Input Clock Frequency (CLK)		110	MHz
TCLK	Input Clock period (CLK)	1/fCLK		ns

Table 9-2:Clock Input Requirements for CLK

Symbol	Parameter	Min	Max	Units
FCLK	Input Clock Frequency (CLK)	2.5	50	MHz
TCLK	Input Clock period (CLK)	1/fCLK		ns

Table 9-3:Clock Input Requirements for crystal oscillator XTAL

Symbol	Parameter	Min	Max	Units
FXTAL	Input Clock Frequency	2.5	10	MHz
TXTAL	Input Clock period	1/fXTAL		ns

9.2 MCU Interface Timing

9.2.1 Parallel 6800-series Interface Timing

Table 9-4: Parallel 6800-series Interface Timing Characteristics (Use CS# as clock)

Symbol	Parameter		Min	Typ	Max	Unit
fMCLK	System Clock Frequency*		1	-	110	MHz
tMCLK	System Clock Period*		1/ fMCLK	-	-	ns
tPWCSH	Control Pulse High Width	Write Read	13 30	1.5* tMCLK 3.5* tMCLK	-	ns
tPWCSL	Control Pulse Low Width	Write (next write cycle) Write (next read cycle) Read	13 80 80	1.5* tMCLK 9* tMCLK 9* tMCLK	-	ns
tAS	Address Setup Time		2	-	-	ns
tAH	Address Hold Time		2	-	-	ns
tDSW	Data Setup Time		4	-	-	ns
tDHW	Data Hold Time		1	-	-	ns
tPLW	Write Low Time		14	-	-	ns
tPHW	Write High Time		14	-	-	ns
tPLWR	Read Low Time		38	-	-	ns
tACC	Data Access Time		32	-	-	ns
tDHR	Output Hold time		1	-	-	ns
tR	Rise Time		-	-	0.5	ns
tF	Fall Time		-	-	0.5	ns

* System Clock denotes external input clock (PLL-bypass) or internal generated clock (PLL-enabled)

Figure 9-1: Parallel 6800-series Interface Timing Diagram (Use CS# as Clock)

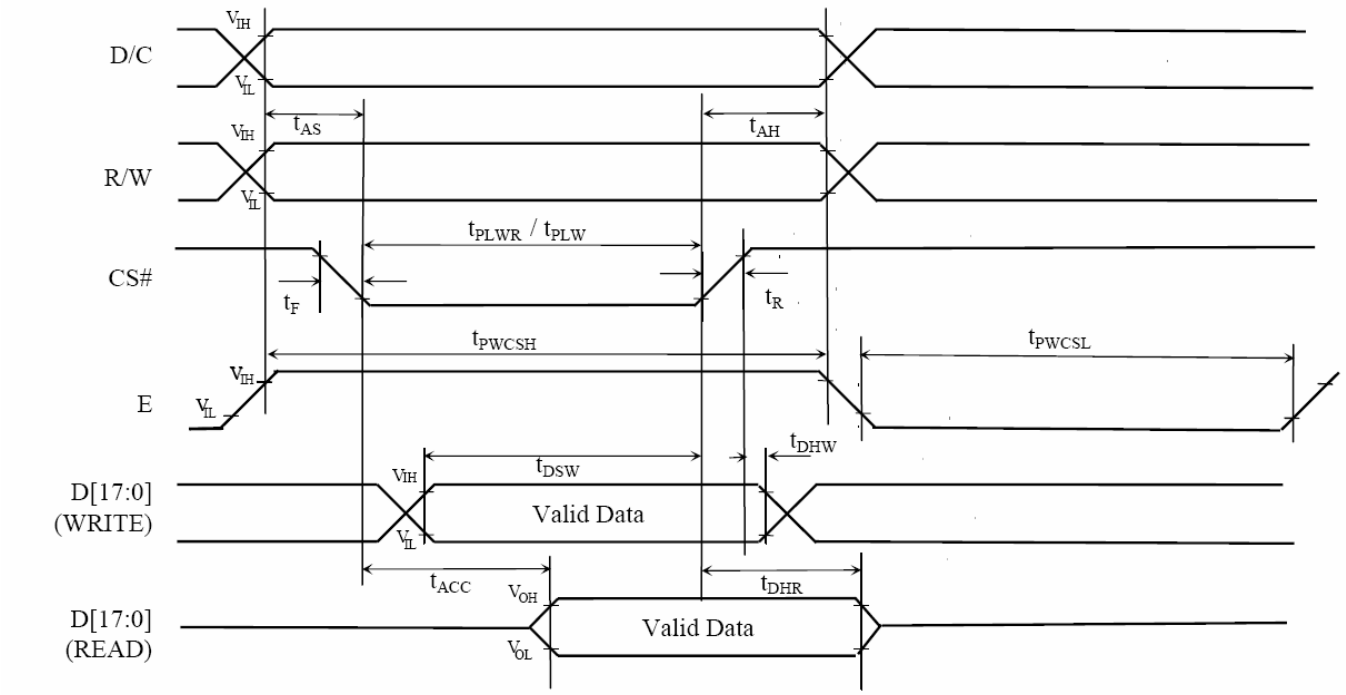
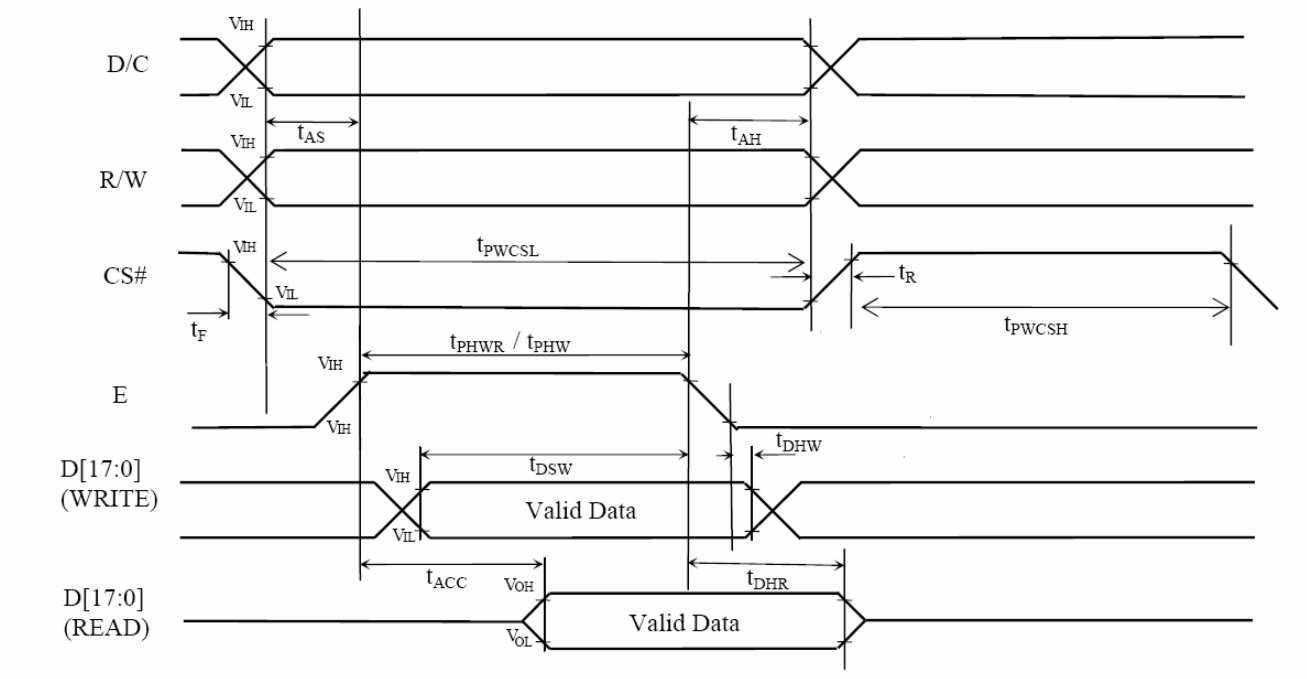


Table 9-5: Parallel 6800-series Interface Timing Characteristics (Use E as clock)

Symbol	Parameter		Min	Typ	Max	Unit
fMCLK	System Clock Frequency*		1	-	110	MHz
tMCLK	System Clock Period*		1/ fMCLK	-	-	ns
tPWCSH	Control Pulse Low Width	Write (next write cycle) Write (next read cycle) Read	13 80 80	1.5* tMCLK 9* tMCLK 9* tMCLK	-	ns
tPWCSL	Control Pulse High Width	Write Read	13 30	1.5* tMCLK 3.5* tMCLK	-	ns
tAS	Address Setup Time		2	-	-	ns
tAH	Address Hold Time		2	-	-	ns
tDSW	Data Setup Time		4	-	-	ns
tDHW	Data Hold Time		1	-	-	ns
tPLW	Write Low Time		14	-	-	ns
tPHW	Write High Time		14	-	-	ns
tPLWR	Read Low Time		38	-	-	ns
tACC	Data Access Time		32	-	-	ns
tDHR	Output Hold time		1	-	-	ns
tR	Rise Time		-	-	0.5	ns
tF	Fall Time		-	-	0.5	ns

* System Clock denotes external input clock (PLL-bypass) or internal generated clock (PLL-enabled)

Figure9-2: Parallel 6800-series Interface Timing Diagram (Use E as Clock)



9.2.2 Parallel 8080-series Interface Timing

Table 9-6: Parallel 8080-series Interface

Symbol	Parameter		Min	Typ	Max	Unit
fMCLK	System Clock Frequency*		1	-	110	MHz
tMCLK	System Clock Period*		1/ fMCLK	-	-	ns
tPWCSL	Control Pulse High Width	Write Read	13 30	1.5* tMCLK 3.5* tMCLK	-	ns
tPWCSH	Control Pulse Low Width	Write (next write cycle) Write (next read cycle) Read	13 80 80	1.5* tMCLK 9* tMCLK 9* tMCLK	-	ns
tAS	Address Setup Time		1	-	-	ns
tAH	Address Hold Time		2	-	-	ns
tDSW	Write Data Setup Time		4	-	-	ns
tDHW	Write Data Hold Time		1	-	-	ns
tPWLW	Write Low Time		12	-	-	ns
tDHR	Read Data Hold Time		1	-	-	ns
tACC	Access Time		32	-	-	ns
tPWLR	Read Low Time		36	-	-	ns
tR	Rise Time		-	-	0.5	ns
tF	Fall Time		-	-	0.5	ns
tCS	Chip select setup time		2	-	-	ns
tCSH	Chip select hold time to read signal		3	-	-	ns

* System Clock denotes external input clock (PLL-bypass) or internal generated clock (PLL-enabled)

Figure 9-3: Parallel 8080-series Interface Timing Diagram (Write Cycle)

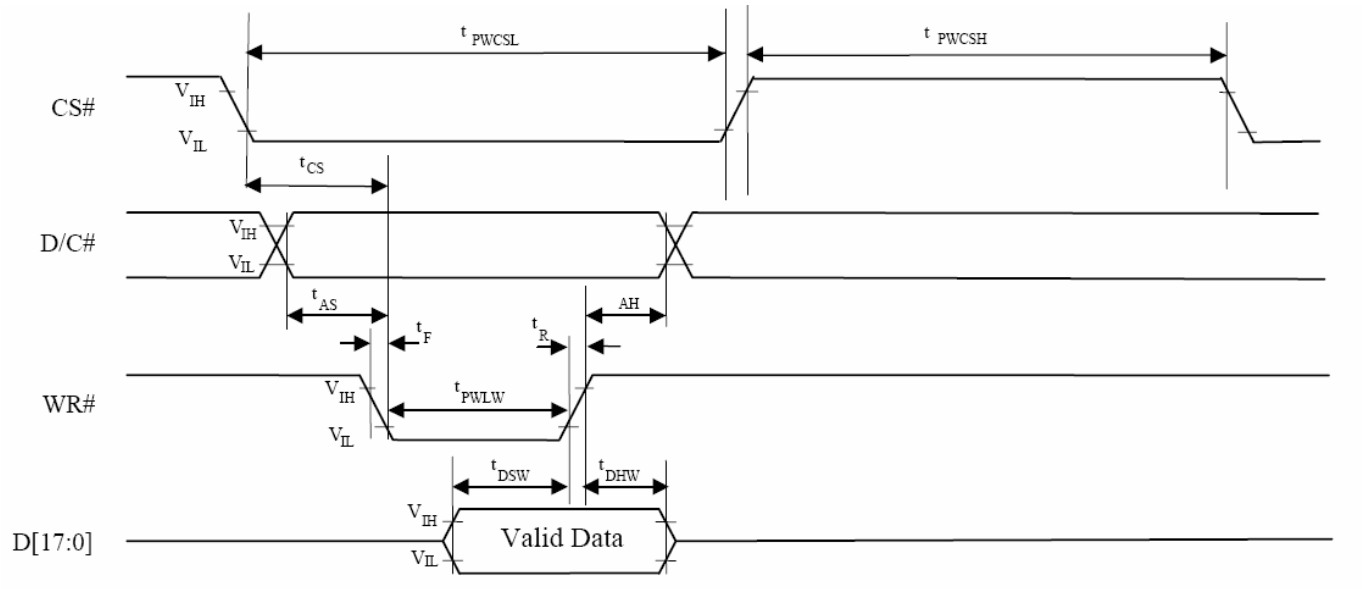
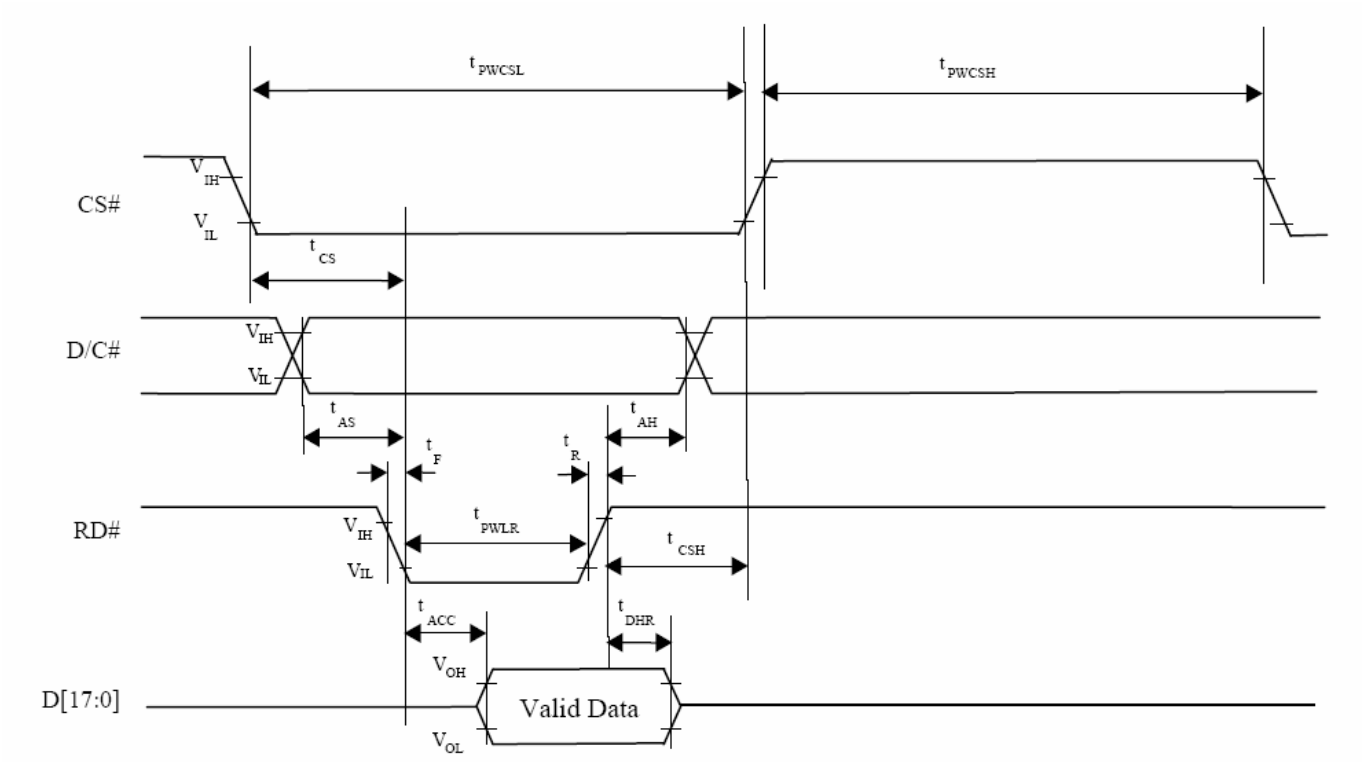


Figure 9-4: Parallel 8080-series Interface Timing Diagram (Read Cycle)



10. Data transfer order Setting

Pixel Data Format

Both 6800 and 8080 support 8-bit, 9-bit, 16-bit, 18-bit and 24-bit data bus. Depending on the width of the data bus, the display data are packed into the data bus in different ways.

Table 8-1: Pixel Data Format

Interface	Cycle	D[23]	D[22]	D[21]	D[20]	D[19]	D[18]	D[17]	D[16]	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
24 bits	1st	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
18 bits	1st							R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
16 bits (565 format)	1st									R5	R4	R3	R2	R1	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1
16 bits	1st									R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0
	2nd									B7	B6	B5	B4	B3	B2	B1	B0	R7	R6	R5	R4	R3	R2	R1	R0
	3rd									G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
12 bits	1st													R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4
	2nd													G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
9 bits	1st																R5	R4	R3	R2	R1	R0	G5	G4	G3
	2nd																G2	G1	G0	B5	B4	B3	B2	B1	B0
8 bits	1st																	R7	R6	R5	R4	R3	R2	R1	R0
	2nd																	G7	G6	G5	G4	G3	G2	G1	G0
	3rd																	B7	B6	B5	B4	B3	B2	B1	B0

11 Register Depiction

Please consult the spec of SSD1963 Version 1.2

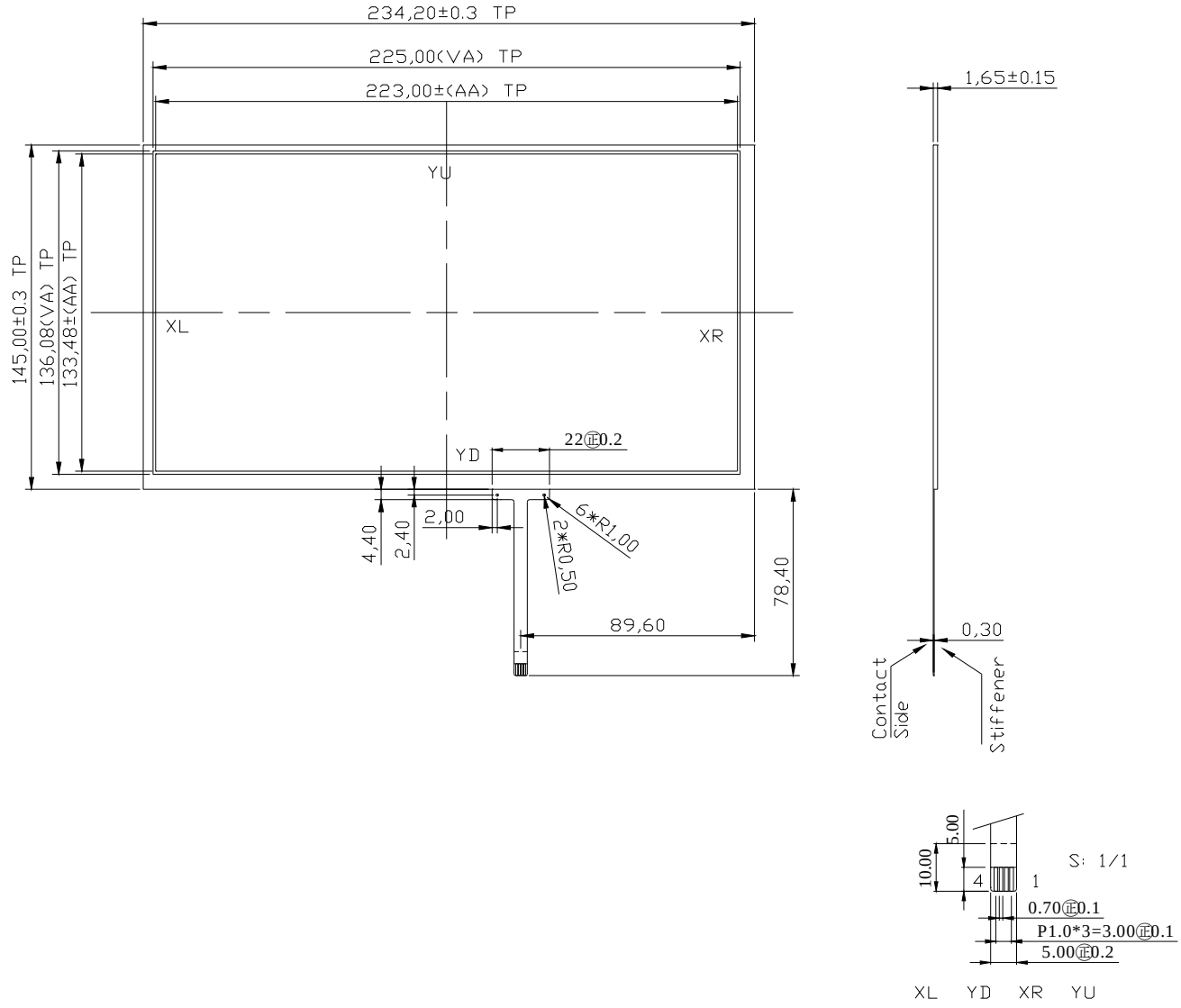
12. LED driving conditions

Item	Symbol	Values			Unit	Remark
		Min.	Typ	Max		
LED forward voltage	V_L	8.4	9.3	10.5	V	Note 1
LED forward current	I_L	180	200	220	mA	
LED life time	-	20,000	-	-	Hr	Note 2

Note 1: The LED Supply Voltage is defined by the number of LED at Ta=25℃ and I_L =200mA.

Note 2: The " LED life time" is defined as the module brightness decrease to 50% original
brightness at Ta=25℃ and I_L =200mA. The LED lifetime could be decreased if operating I_L is larger than 200 mA.

13. Touch panel Information



Non-Proper Ways to handle the touch screen

1. Do not pull or crease the tail of the touch screen.
2. Tails, unless the drawing calls out for a bend, are to be free of permanent creases in the polyester, slight crease lines in the adhesive tail cover are allowed

.

14.Reliability Test

WIDE TEMPERATURE RELIABILITY TEST

NO.	ITEM	CONDITION			STANDARD	NOTE
1	High Temp. Storage	85℃	240 Hrs		Appearance without defect	
2	Low Temp. Storage	-30℃	240 Hrs		Appearance without defect	
3	High Temp. & High Humidity. Storage	60 ℃ 90%RH	240 Hrs		Appearance without defect	
4	High Temp. Operating Display	70℃	240 Hrs		Appearance without defect	
5	Low Temp. Operating Display	-20℃	240 Hrs		Appearance without defect	
6	Thermal Shock	-20 ℃, 30min. →70℃, 30min. (1cycle)			Appearance without defect	100 cycles

Inspection Provision

1.Purpose

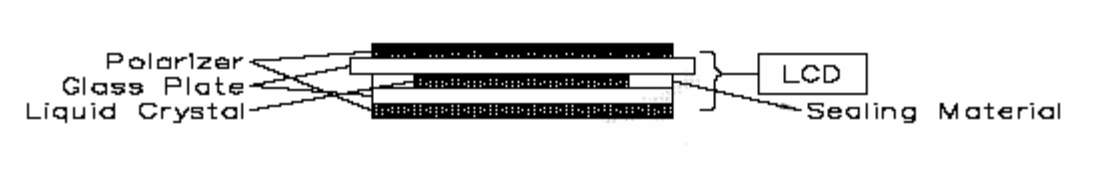
The WINSTAR inspection provision provides outgoing inspection provision and its expected quality level based on our outgoing inspection of WINSTAR LCD produces.

2.Applicable Scope

The WINSTAR inspection provision is applicable to the arrangement in regard to outgoing inspection and quality assurance after outgoing.

3.Technical Terms

3-1 WINSTAR Technical Terms



4.Outgoing Inspection

4-1 Inspection Method

MIL-STD-105E Level Ⅱ Regular inspection

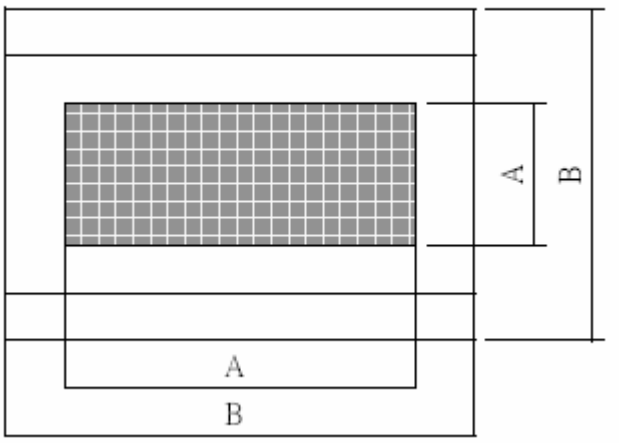
4-2 Inspection Standard

	Item		AQL(%)	Remarks
Major Defect	Dots	Opens Shorts Erroneous operation	0.4	Faults which substantially lower the practicality and the initial purpose difficult to achieve
	Solder appearance	Shorts Loose		
	Cracks	Display surface cracks		
	Dimensions	External from Dimensions	0.4	
Minor Defect	Inside the glass	Black spots	0.65	Faults which appear to pose almost no obstacle to the practicality, effective use, and operation
	Polarizing plate	Scratches, foreign Matter, air bubbles, and peeling		
	Dots	Pinhole, deformation		
	Color tone	Color unevenness		
	Solder appearance	Cold solder Solder projections		

4-3 Inspection Provisions

*Viewing Area Definition

Fig. 1



A : Zone Viewing Area

B : Zone Glass Plate Outline

*Inspection place to be 500 to 1000 lux illuminance uniformly without glaring.
The distance between luminous source(daylight fluorescent lamp and cool white fluorescent lamp) and sample to be 30 cm to 50 cm.

*Test and measurement are performed under the following conditions, unless otherwise specified.

Temperature 20 ± 15℃

Humidity 65 ± 20%R.H.

Pressure 860~1060hPa(mmbar)

In case of doubtful judgment, it is performed under the following conditions.

Temperature 20 ± 2℃

Humidity 65 ±5%R.H.

Pressure 860~1060hPa(mmbar)

5.Specification for quality check

5-1-1 Electrical characteristics :

NO.	Item	Criterion
1	Non operational	Fail
2	Miss operating	Fail
3	Contrast irregular	Fail
4	Response time	Within Specified value

5-1-2 Components soldering :

Should be no defective soldering such as shorting, loose terminal cold solder, peeling of printed circuit board pattern, improper mounting position, etc.

5-2 Inspection Standard for TFT panel

5-2-1 The environmental condition of inspection :

The environmental condition and visual inspection shall be conducted as below.

(1) Ambient temperature : 25±5℃

(2) Humidity : 25~75% RH

(3) External appearance inspection shall be conducted by using a single 20W fluorescent lamp or equivalent illumination.

(4) Visual inspection on the operation condition for cosmetic shall be conducted at the distance 30cm or more between the LCD panels and eyes of inspector. The viewing angle shall be 90 degreeto the front surface of display panel.

(5) Ambient Illumination : 300~500 Lux for external appearance inspection.

(6) Ambient Illumination : 100~200 Lux for light on inspection.

5-2-2 Inspection Criteria

(1) Definition of dot defect induced from the panel inside

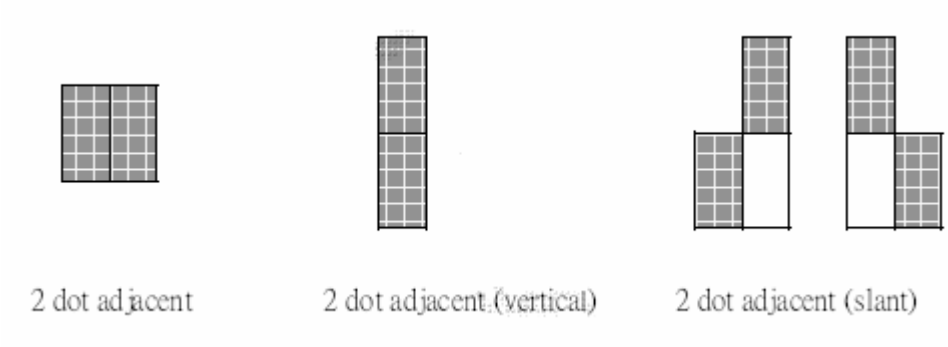
a) The definition of dot : The size of a defective dot over 1/2 of whole dot is regarded as one defective dot

b) Bright dot : Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

c) Dark dot : Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue pattern.

d) 2 dot adjacent = 1 pair = 2 dots

Picture :



(2) Display Inspection

NO.	Item			Acceptable Count
1	Dot defect	Bright Dot	Random	N ≦ 2
			2 dots adjacent	N ≦ 0
		Dark Dot	Random	N ≦ 3
			2 dots adjacent	N ≦ 1
		Total bright and dark dot		N ≦ 4
	Functional failure (V-line/ H-line/Cross line etc.)			Not allowable
	Mura	It's OK if mura is slight visible through 6% ND filter. (Judged by limit sample if it is necessary)		
2	Newton ring (touch panel)	Orbicular of interference fringes is not allowed in the optimum contrast within the active area under viewing angle.		

(3) Appearance inspection

NO.	Item	Standards
1	Panel Crack	Not allow. It is shown in Fig.1.
2	Broken CF Non -lead Side of TFT	The broken in the area of W > 2mm is ignored, L is ignored. It is shown in Fig.2.
3	Broken Lead Side of TFT	FPC lead, electrical line or alignment mark can't be damaged. It is shown in Fig.3.
4	Broken Corner of TFT at Lead Side	FPC lead. electrical line or alignment mark can't be damaged. It is shown in Fig.4.
5	Burr of TFT / CF Edge	The distance of burr from the edge of TFT / CF, W ≦ 0.3mm. It is shown in Fig.5.
6	Foreign Black / White/Bright Spot	(1) 0.15 < D ≦ 0.5 mm, N≦ 4 ; (2) D ≦ 0.15mm, Ignore. It is shown in Fig.6.
7	Foreign Black / White/Bright Line	(1) 0.05<W≦ 0.1 mm, 0.3<L≦2 mm, N≦ 4.
		(2) W ≦ 0.05mm and L≦ 0.3mm Ignore.
		It is shown in Fig.7.
8	Color irregular	Not remarkable color irregular.

Fig 1.

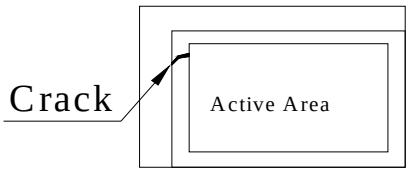


Fig 2.

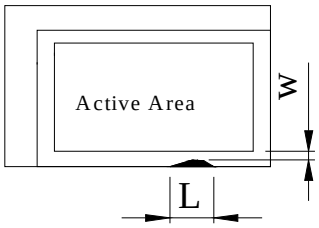


Fig 3.

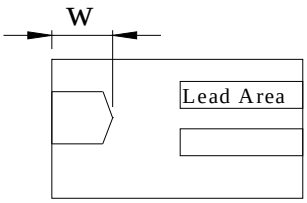


Fig 4.

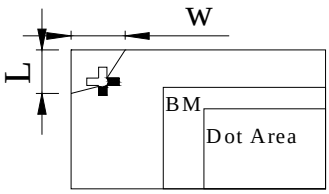


Fig 5.

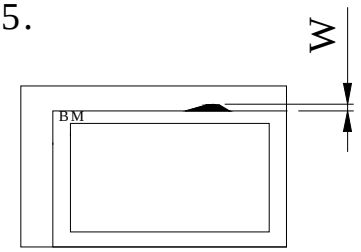
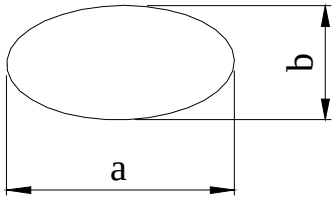


Fig 6.



D=(a+b)/2

Fig 7.

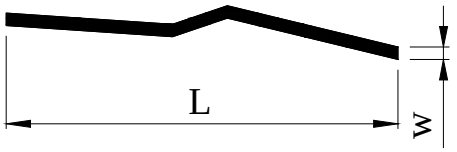
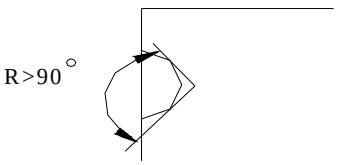


Fig8.



Notes
1.W:Widh
2.Lengh
3.D:Average Diameter
4.N:Count
5.All the anhle of the broken must be larger than 90～.It is shown in Fig.8.(R>90～)

NOTICE:

- SAFETY

1. If the LCD panel breaks, be careful not to get the liquid crystal to touch your skin.
2. If the liquid crystal touches your skin or clothes, please wash it off immediately by using soap and water.

- HANDLING

1. Avoid static electricity which can damage the CMOS LSI.
2. Do not remove the panel or frame from the module.
3. The polarizing plate of the display is very fragile. So, please handle it very carefully.
4. Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the surface of plate.
5. Do not use ketonics solvent & Aromatic solvent. Use a soft cloth soaked with a cleaning naphtha solvent.

- STORAGE

1. Store the panel or module in a dark place where the temperature is 25±5℃ and the humidity is below 65% RH.
2. Do not place the module near organics solvents or corrosive gases.
3. Do not crush, shake, or jolt the module.

- TERMS OF WARRANT

1. Acceptance inspection period

The period is within one month after the arrival of contracted commodity at the buyer's factory site.

2. Applicable warrant period

The period is within twelve months since the date of shipping out under normal using and storage conditions.