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SPECIFICATION

CUSTOMER : _____

MODULE NO.: WF102ATIFGDBN0#

APPROVED BY: **(FOR CUSTOMER USE ONLY)**	**PCB VERSION:** **DATA:**

SALES BY	APPROVED BY	CHECKED BY	PREPARED BY

VERSION	DATE	REVISED PAGE NO.	SUMMARY
0	2013.04.09		First issue

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華凌光電股份有限公司

MODLE NO：

DOC. FIRST ISSUE

RECORDS OF REVISION

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Contents

1.Module Classification Information

W	F	102	A	T	I	F	G	D	B	N	0	#
①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩	⑪	⑫	⑬

① Brand：WINSTAR DISPLAY CORPORATION
② Display Type：H→Character Type, G→Graphic Type F→TFT Type
③ Display Size：10.2” TFT
④ Model serials no.
⑤ Backlight Type： F→CCFL, White T→LED, White
S→LED, High Light White

⑥ LCD Polarize Type/ Temperature range/ Gray Scale Inversion Direction
I→Transmissive, W. T, 6:00
L→Transmissive, W.T,12:00

⑦ A：TFT LCD
B：TFT+FR+CONTROL BOARD
C：TFT+FR+A/D BOARD
D：TFT+FR+A/D BOARD+CONTROL BOARD
E：TFT+FR+POWER BOARD
F：TFT+CONTROL BOARD
G：TFT+FR
H：TFT+D/V BOARD
I：TFT+FR+D/V BOARD
J：TFT+POWER BD

⑧ Solution:
A: 128160 B:320234 C:320240 D:480234 E:480272 F: 640480 G: 800480
H:1024600 I:320480 J:240320 K:800600 L:240400 M :1024768

⑨ D: Digital L：LVDS

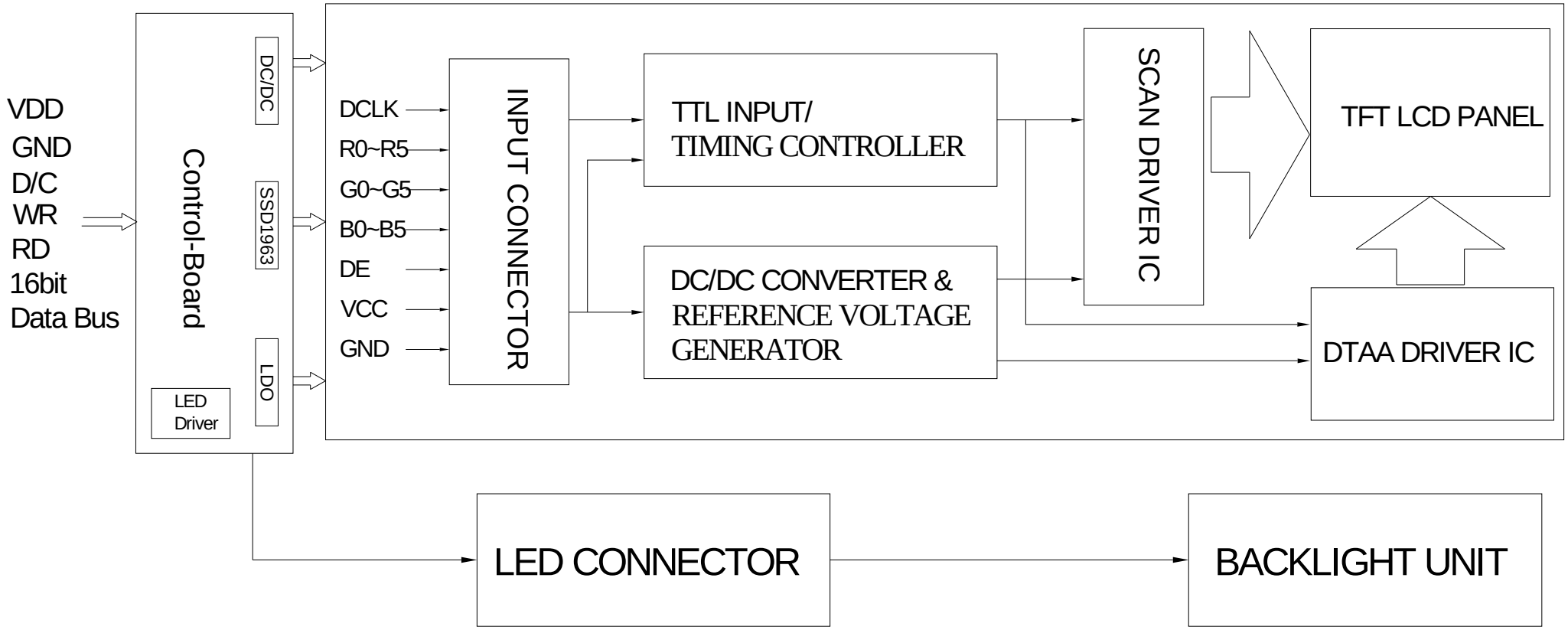
⑩ Interface： N：without control board A：8Bit B：16Bit

⑪ TS： N：Without TS T：resistive touch panel C：capacitive touch panel
⑫ Version
⑬ Special Code #:Fit in with ROHS directive regulations

2.General Specification

Parameter		Specifications	Unit
LCD size		10.2(Diagonal)	Inch
Display mode		Normally white, Transmissive type	
Number of Pixel		800 RGB x 480	Dot
Active area		222.0(W) × 132.48(H)	mm
Pixel Pitch		0.0925(W) × 0.276(H)	mm
Pixel Configuration		RGB-Stripe	
View Direction		12 o'clock	
Gray Scale Inversion Direction		6 o'clock	
Outline Dimension		235.0 (H) x145.0 (V) x 10.2 (D)	mm
Controller IC		SSD1963	
Interface		Digital 8080 family MPU	
Temperature Range	Operation	-30~85	^{0}C
	Storage	-30~85	^{0}C

3.Block Diagram



4.Electrical Characteristics

4-1. ELECTRICAL CHARACTERISTICS OF LCM

ITEM	SYMBOL	CONDITION	MIN.	TYPICAL	MAX.	UNIT
Digital Power Supply Voltages	V_{DD}	V_{DD} -DGND	3.0	3.3	3.6	V
Digital Supply Current Consumption	I_{VDD}	V_{DD}=3.3V	900	1150	1200	mA
Build-in DC/DC for LED B/L	I_{LED}		180	200	220	mA
Build-in DC/DC for LED B/L	V_{LED}		8.4	9.3	10.5	V
Input Logic Signal High Threshold	VIH		0.7 V_{DD}	-	V_{DD}	V
Input Logic Signal Low Threshold	VIL		0	-	0.3 V_{DD}	V
Brightness	L	White Pattern	-	350	-	cd/m2
LED life time	-	I_{LED}=200mA	20,000	-	-	Hr

＊ Recommended TFT Driving for 25℃

＊ The LED Supply Voltage is defined by the number of LED at Ta=25℃ and I_L =200mA.

＊ The " LED life time" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and I_L =200mA. The LED lifetime could be decreased if operating I_L is larger than 200 mA.

5.Absolute Maximum Ratings

Item	Symbol	Values		Unit	Remark
		Min	Max		
Power voltage	VCC	-0.3	5	V	
Operation temperature	TOP	-30	85	°C	
Storage temperature	TST	-30	85	°C	
LED Reverse Voltage	VR	-	1.2	V	Each LED Note 1
LED Forward Current	IF	-	25	MA	Each LED

Note 1: Vr conditions: Zener Diode 20mA.

6.Interface Pin Function

LCM PIN Definition

P/N	Symbol	16 B IT Function
1	VDD	Power supply for Logic
2	VDD	Power supply for Logic
3-18	DB0-DB15	16Bits Data bus
19	CS	Chip select
20	D/C	Command/Data select
21	WR	8080 family MPU interface : Write signal
22	RD	8080 family MPU interface: Read signal
23	NC	No connection
24	RST	Reset
25	NC	No connection
26	NC	No connection
27	NC	No connection
28	NC	No connection
29	NC	No connection
30	NC	No connection
31	NC	No connection
32	GND	Ground

LED BACKLIGHT (J1): JST BHSR-02VS-1

Pin No.	Symbol
1	A
2	K

CORRESPONDABLE BACKLIGHT CONNECTOR : SM 02B-BHSS-1

7.Electro-optical Characteristics

Item		Symbol	Condition	Min	Typ	Max	Unit	Note
Response time		T_{ON}	θ=0°	-	15	30	ms	Note 3
		T_{OFF}		-	20	40	ms	
Contrast ratio		CR		250	300	-	-	Note 4
Color Chromaticity	White	Wx		0.26	0.31	0.36	%	Note 2,5,6
		Wy		0.28	0.33	0.38		
Viewing Angle	Hor.	θR	θ=180°	55	65	-	Degree	Note 1
		θL	θ=0°	55	65	-		
	Ver.	θT	θ=90°	35	45	-		
		θB	θ=2700°	55	65	-		
Luminance		L	θ=0°	280	350	-	cd/m2	Note 6
Luminance uniformity		Y_U	θ=0°	70	75		%	Note 7

Test Conditions:

1. V_{CC}=3.3V, I_L=200mA (Backlight current), the ambient temperature is 25℃.
2. The test systems refer to Note 2.

Note 1: Definition of viewing angle range

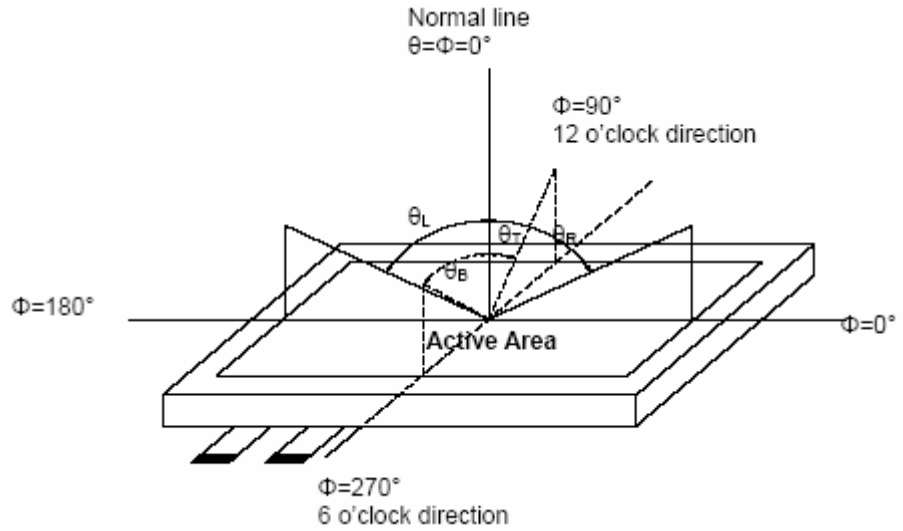


Fig. 4-1 Definition of viewing angle

Note 2: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 30 minutes operation, the optical properties are measured at the center point of the LCD screen. (Response time is measured by Photo detector TOPCON BM-7, other items are measured by BM-5A/Field of view: 1° /Height: 500mm.)

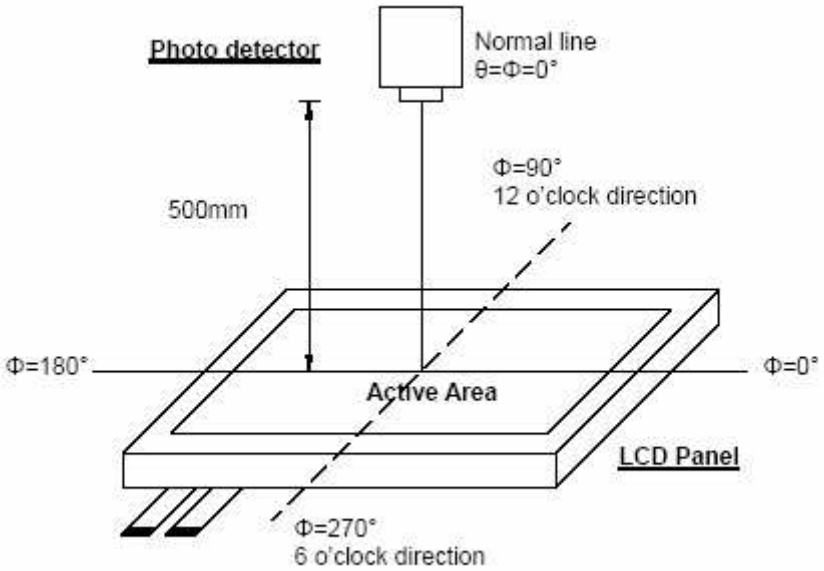


Fig. 4-2 Optical measurement system setup

Note 3: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.

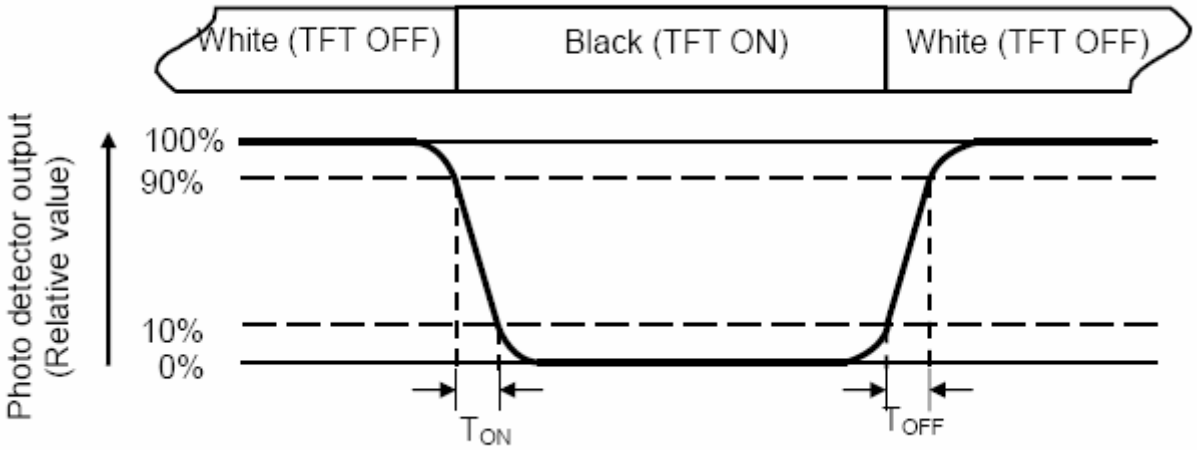


Fig. 4-3 Definition of response time

Note 4: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6: All input terminals LCD panel must be ground when measuring the center area of the panel. The LED driving condition is I_L=200mA.

Note 7: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer to Fig. 4-4).Every measuring point is placed at the center of each measuring area.

$$\textit{Luminance Uniformity (Yu)} = \frac{B_{min}}{B_{max}}$$

L-------Active area length W----- Active area width

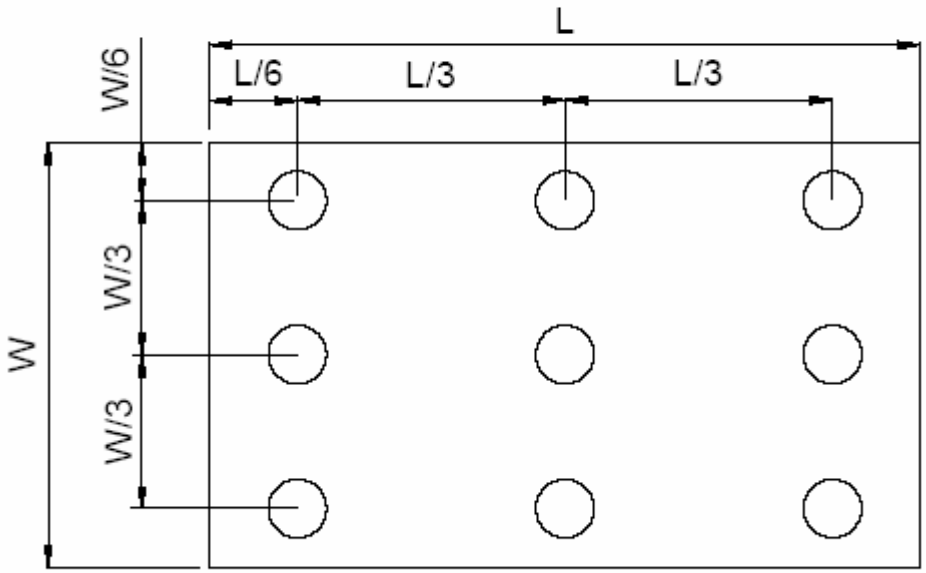
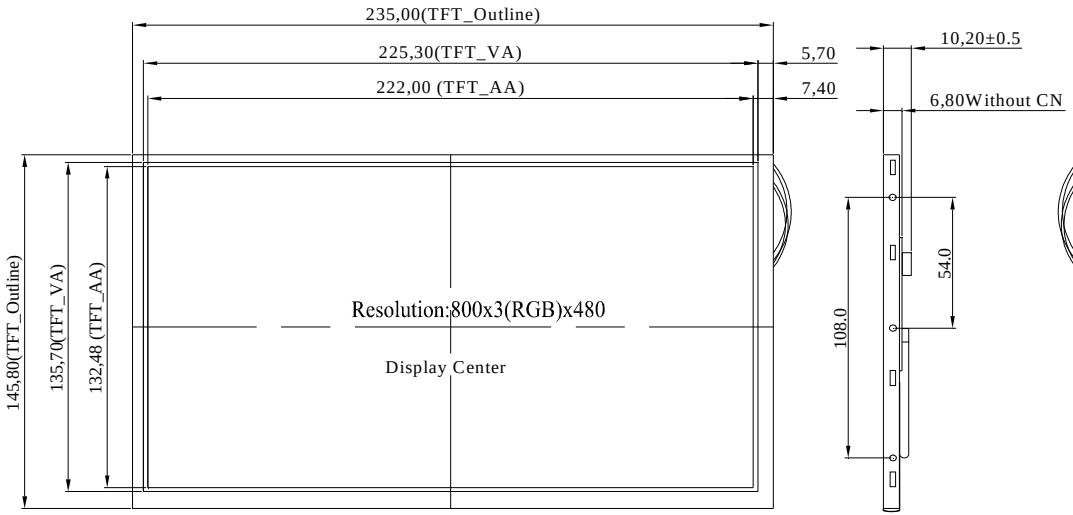


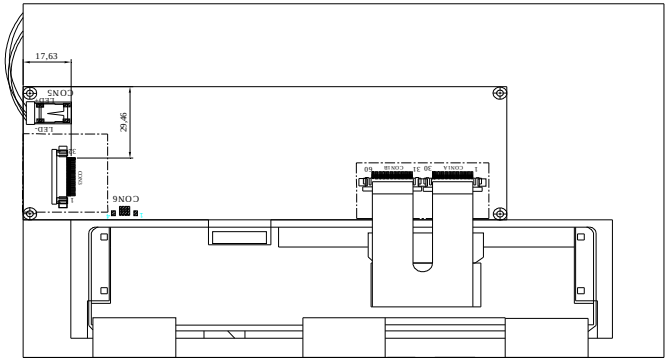
Fig. 4-4 Definition of measuring points

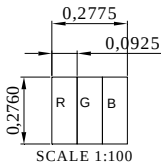
B_{max}: The measured maximum luminance of all measurement position.

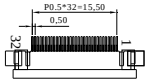
B_{min}: The measured minimum luminance of all measurement position.

8. Contour Drawing









PIN NO.	SYMBOL
1	VDD
2	VDD
3	DB0
4	DB1
5	DB2
6	DB3
7	DB4
8	DB5
9	DB6
10	DB7
11	DB8
12	DB9
13	DB10
14	DB11
15	DB12
16	DB13
17	DB14
18	DB15
19	CS
20	D/C
21	RD
22	WR
23	NC
24	RST
25	NC
26	NC
27	NC
28	NC
29	NC
30	NC
31	NC
32	GND

The non-specified tolerance of dimension is ±0.3mm.

9. AC Characteristics

Conditions:

Voltage referenced to VSS

VDDD, VDDPLL = 1.2V

VDDIO, VDDLCD = 3.3V

TA = 25°C

CL = 50pF (Bus/CPU Interface)

CL = 0pF (LCD Panel Interface)

9.1 Clock Timing

Table 9-1:Clock Input Requirements for CLK (PLL-bypass)

Symbol	Parameter	Min	Max	Units
FCLK	Input Clock Frequency (CLK)		110	MHz
TCLK	Input Clock period (CLK)	1/fCLK		ns

Table 9-2:Clock Input Requirements for CLK

Symbol	Parameter	Min	Max	Units
FCLK	Input Clock Frequency (CLK)	2.5	50	MHz
TCLK	Input Clock period (CLK)	1/fCLK		ns

Table 9-3:Clock Input Requirements for crystal oscillator XTAL

Symbol	Parameter	Min	Max	Units
FXTAL	Input Clock Frequency	2.5	10	MHz
TXTAL	Input Clock period	1/fXTAL		ns

9.2 MCU Interface Timing

9.2.1 Parallel 6800-series Interface Timing

Table 9-4: Parallel 6800-series Interface Timing Characteristics (Use CS# as clock)

Symbol	Parameter		Min	Typ	Max	Unit
fMCLK	System Clock Frequency*		1	-	110	MHz
tMCLK	System Clock Period*		1/ fMCLK	-	-	ns
tPWCSH	Control Pulse High Width	Write Read	13 30	1.5* tMCLK 3.5* tMCLK	-	ns
tPWCSL	Control Pulse Low Width	Write (next write cycle) Write (next read cycle) Read	13 80 80	1.5* tMCLK 9* tMCLK 9* tMCLK	-	ns
tAS	Address Setup Time		2	-	-	ns
tAH	Address Hold Time		2	-	-	ns
tDSW	Data Setup Time		4	-	-	ns
tDHW	Data Hold Time		1	-	-	ns
tPLW	Write Low Time		14	-	-	ns
tPHW	Write High Time		14	-	-	ns
tPLWR	Read Low Time		38	-	-	ns
tACC	Data Access Time		32	-	-	ns
tDHR	Output Hold time		1	-	-	ns
tR	Rise Time		-	-	0.5	ns
tF	Fall Time		-	-	0.5	ns

* System Clock denotes external input clock (PLL-bypass) or internal generated clock (PLL-enabled)

Figure 9-1: Parallel 6800-series Interface Timing Diagram (Use CS# as Clock)

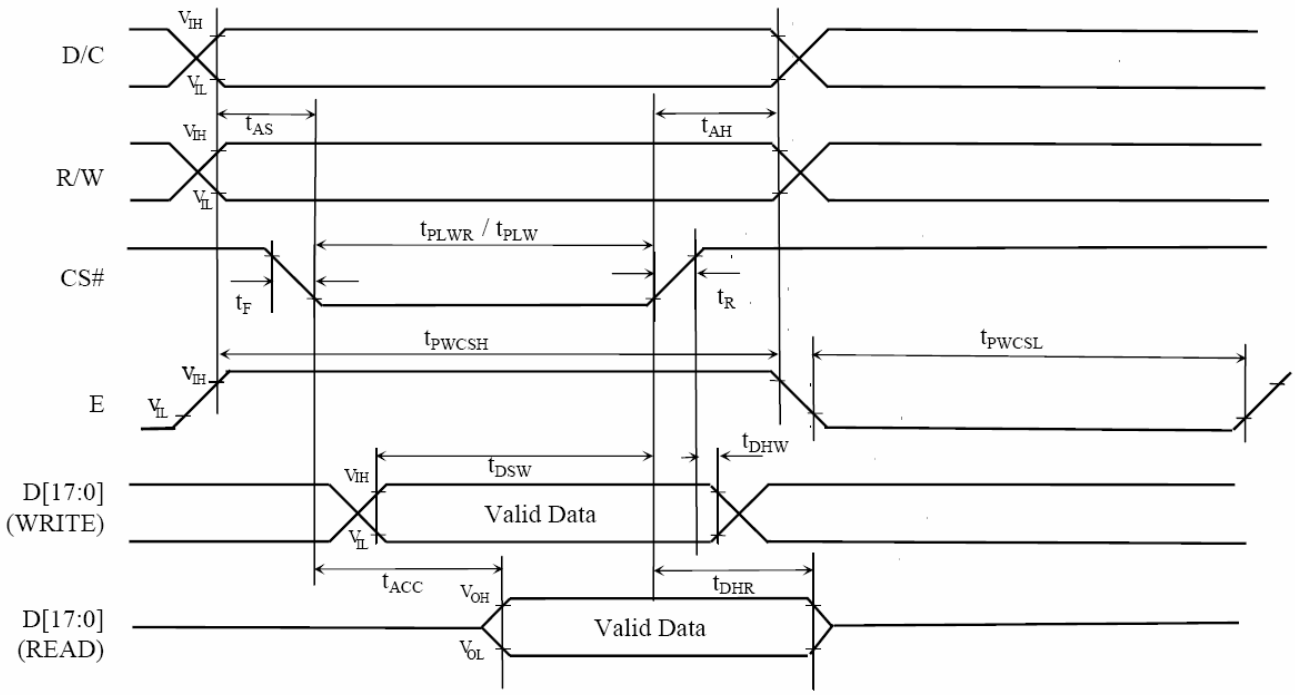
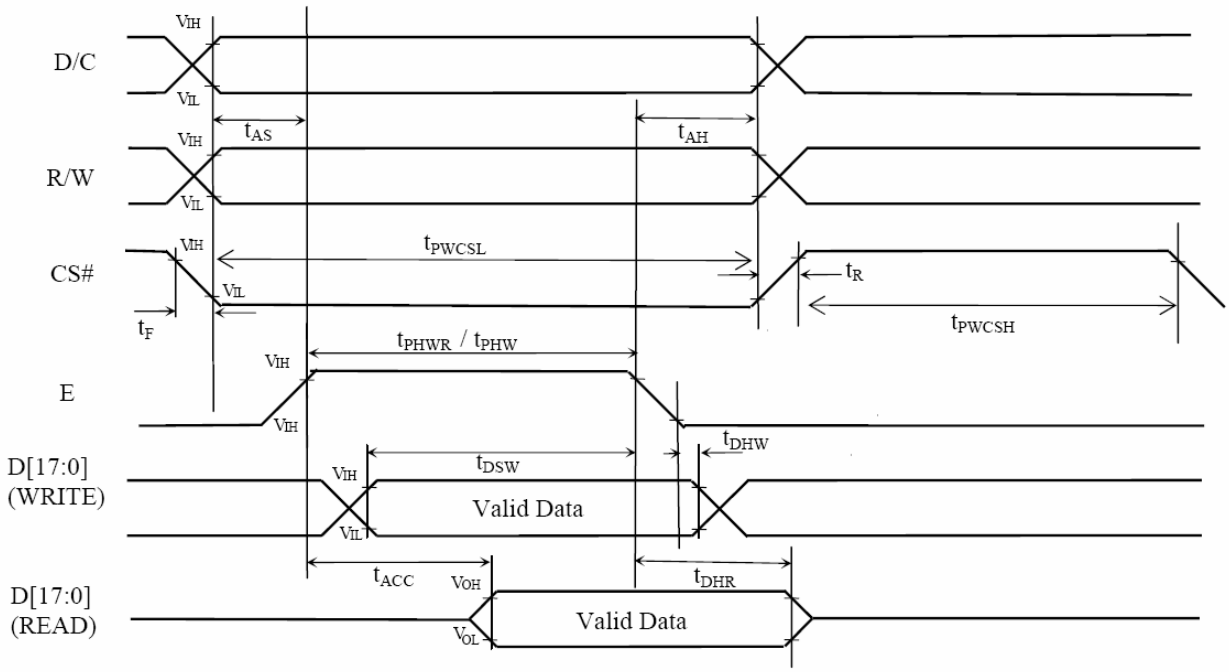


Table 9-5: Parallel 6800-series Interface Timing Characteristics (Use E as clock)

Symbol	Parameter		Min	Typ	Max	Unit
fMCLK	System Clock Frequency*		1	-	110	MHz
tMCLK	System Clock Period*		1/ fMCLK	-	-	ns
tPWCSH	Control Pulse Low Width	Write (next write cycle) Write (next read cycle) Read	13 80 80	1.5* tMCLK 9* tMCLK 9* tMCLK	-	ns
tPWCSL	Control Pulse High Width	Write Read	13 30	1.5* tMCLK 3.5* tMCLK	-	ns
tAS	Address Setup Time		2	-	-	ns
tAH	Address Hold Time		2	-	-	ns
tDSW	Data Setup Time		4	-	-	ns
tDHW	Data Hold Time		1	-	-	ns
tPLW	Write Low Time		14	-	-	ns
tPHW	Write High Time		14	-	-	ns
tPLWR	Read Low Time		38	-	-	ns
tACC	Data Access Time		32	-	-	ns
tDHR	Output Hold time		1	-	-	ns
tR	Rise Time		-	-	0.5	ns
tF	Fall Time		-	-	0.5	ns

* System Clock denotes external input clock (PLL-bypass) or internal generated clock (PLL-enabled)

Figure9-2: Parallel 6800-series Interface Timing Diagram (Use E as Clock)



9.2.2 Parallel 8080-series Interface Timing

Table 9-6: Parallel 8080-series Interface

Symbol	Parameter		Min	Typ	Max	Unit
fMCLK	System Clock Frequency*		1	-	110	MHz
tMCLK	System Clock Period*		1/ fMCLK	-	-	ns
tPWCSL	Control Pulse High Width	Write Read	13 30	1.5* tMCLK 3.5* tMCLK	-	ns
tPWCSH	Control Pulse Low Width	Write (next write cycle) Write (next read cycle) Read	13 80 80	1.5* tMCLK 9* tMCLK 9* tMCLK	-	ns
tAS	Address Setup Time		1	-	-	ns
tAH	Address Hold Time		2	-	-	ns
tDSW	Write Data Setup Time		4	-	-	ns
tDHW	Write Data Hold Time		1	-	-	ns
tPWLW	Write Low Time		12	-	-	ns
tDHR	Read Data Hold Time		1	-	-	ns
tACC	Access Time		32	-	-	ns
tPWLR	Read Low Time		36	-	-	ns
tR	Rise Time		-	-	0.5	ns
tF	Fall Time		-	-	0.5	ns
tCS	Chip select setup time		2	-	-	ns
tCSH	Chip select hold time to read signal		3	-	-	ns

* System Clock denotes external input clock (PLL-bypass) or internal generated clock (PLL-enabled)

Figure 9-3: Parallel 8080-series Interface Timing Diagram (Write Cycle)

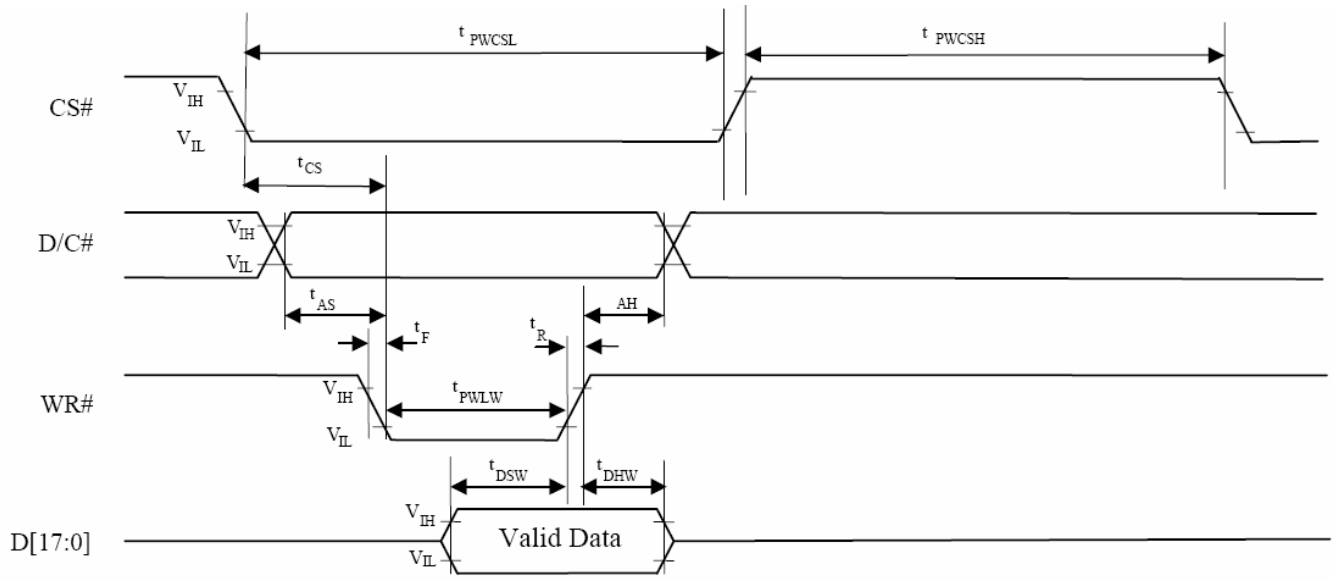
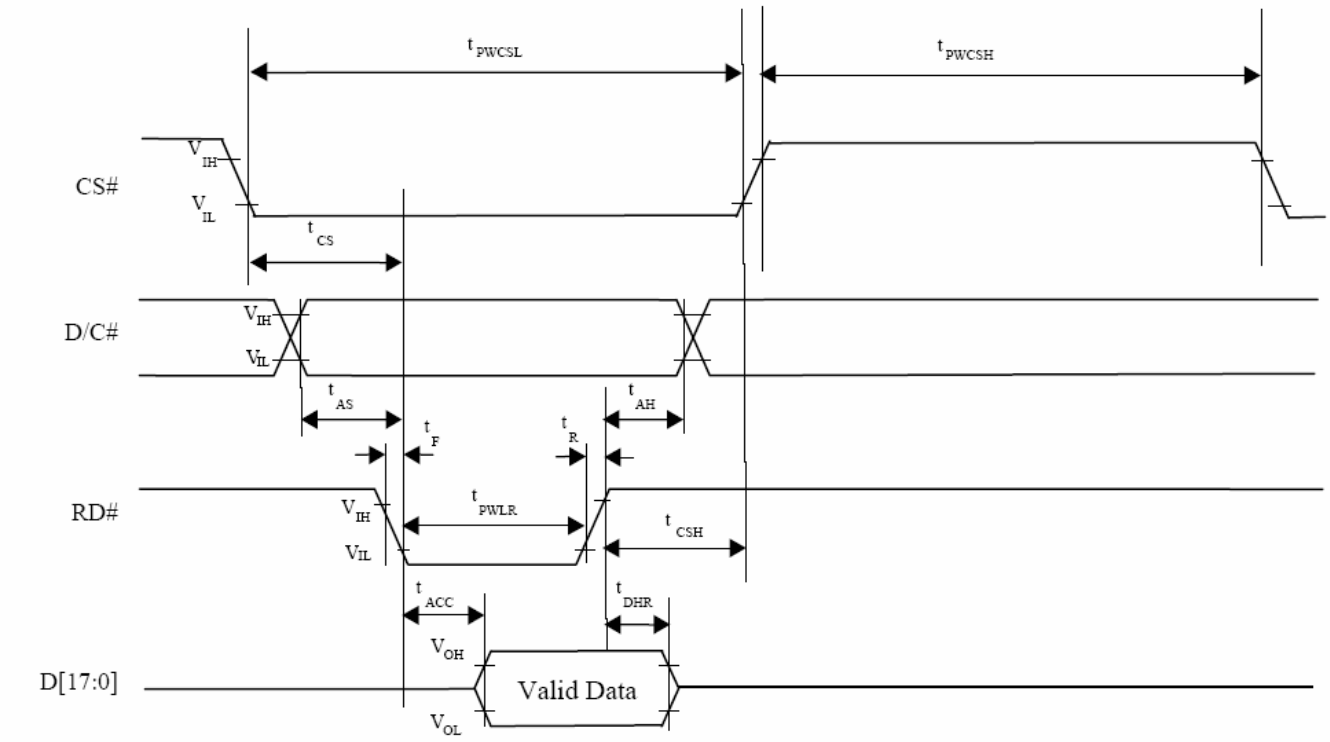


Figure 9-4: Parallel 8080-series Interface Timing Diagram (Read Cycle)



10. Data transfer order Setting

Pixel Data Format

Both 6800 and 8080 support 8-bit, 9-bit, 16-bit, 18-bit and 24-bit data bus. Depending on the width of the data bus, the display data are packed into the data bus in different ways.

Table 8-1: Pixel Data Format

Interface	Cycle	D[23]	D[22]	D[21]	D[20]	D[19]	D[18]	D[17]	D[16]	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
24 bits	1st	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
18 bits	1st							R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
16 bits (565 format)	1st									R5	R4	R3	R2	R1	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1
16 bits	1st									R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0
	2nd									B7	B6	B5	B4	B3	B2	B1	B0	R7	R6	R5	R4	R3	R2	R1	R0
	3rd									G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
12 bits	1st													R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4
	2nd													G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
9 bits	1st																R5	R4	R3	R2	R1	R0	G5	G4	G3
	2nd																G2	G1	G0	B5	B4	B3	B2	B1	B0
8 bits	1st																	R7	R6	R5	R4	R3	R2	R1	R0
	2nd																	G7	G6	G5	G4	G3	G2	G1	G0
	3rd																	B7	B6	B5	B4	B3	B2	B1	B0

11 Register Depiction

Please consult the spec of SSD1963 Version 1.2

12.Reliability Test

Content of Reliability Test (Wide temperature, -30℃~85℃)

Environmental Test			
Test Item	**Content of Test**	**Test Condition**	**Note**
High Temperature storage	Endurance test applying the high storage temperature for a long time.	85℃ 200hrs	2
Low Temperature storage	Endurance test applying the high storage temperature for a long time.	-30℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	85℃ 200hrs	——
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-30℃ 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max For 96hrs under no-load condition excluding the polarizer, Then taking it out and drying it at normal temperature.	60℃,90%RH 96hrs	1,2
Thermal shock resistance	The sample should be allowed stand the following 10 cycles of operation -30℃ 25℃ 85℃ 30min 5min 30min 1 cycle	-30℃/85℃ 10 cycles	——
Vibration test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude : 15mm Vibration Frequency : 10~55Hz One cycle 60 seconds to 3 directions of X,Y,Z for Each 15 minutes	3
Static electricity test	Endurance test applying the electric stress to the terminal.	VS=800V,RS=1.5kΩ CS=100pF 1 time	——

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal Temperature and humidity after remove from the test chamber.

Note3: Vibration test will be conducted to the product itself without putting it in a container.