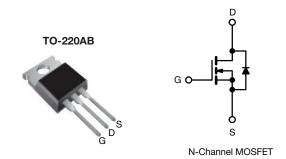
Vishay Siliconix

Power MOSFET

PRODUCT SUMMA	RY	
V _{DS} (V)	20	00
$R_{DS(on)}(\Omega)$	V _{GS} = 10 V	0.18
Q _g (Max.) (nC)	7	0
Q _{gs} (nC)	1	3
Q _{gd} (nC)	3	9
Configuration	Sin	gle



FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- · Fast switching
- · Ease of paralleling
- Simple drive requirements
- · Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Note

This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION	
Package	TO-220AB
Lood (Ph) from	IRF640PbF
Lead (Pb)-free	SiHF640-E3
SnPb	IRF640
SIPO	SiHF640

PARAMETER		SYMBOL	LIMIT	UNIT		
Drain-Source Voltage		V _{DS}	200	.,		
Gate-Source Voltage		V_{GS}	± 20	V		
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C T _C = 100 °C		18		
Continuous Drain Current	V _{GS} at 10 V	T _C = 100 °C	'D	I _D 11		
Pulsed Drain Current ^a			I _{DM}	72		
Linear Derating Factor			1.0	W/°C		
Single Pulse Avalanche Energy b		E _{AS}	580	mJ		
Repetitive Avalanche Current ^a			I _{AR}	18	Α	
Repetitive Avalanche Energy ^a		E _{AR}	13	mJ		
Maximum Power Dissipation $T_C = 25 ^{\circ}C$		P_D	125	W		
Peak Diode Recovery dV/dt ^c		dV/dt	5.0	V/ns		
Operating Junction and Storage Temperature Rang	е		T _J , T _{stg}	-55 to +150	°C	
Soldering Recommendations (Peak temperature) ^d	ndations (Peak temperature) d for 10 s 300					
Mounting Toyaus	10 lbf	lbf ⋅ in				
Mounting Torque	6-32 or M3 screw			1.1	N⋅m	

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11). b. $V_{DD}=50$ V, starting $T_J=25$ °C, L=2.7 mH, $R_g=25$ Ω , $I_{AS}=18$ A (see fig. 12). c. $I_{SD}\leq 18$ A, $dI/dt\leq 150$ A/µs, $V_{DD}\leq V_{DS}$, $T_J\leq 150$ °C. d. 1.6 mm from case.



Vishay Siliconix

THERMAL RESISTANCE RATI	NGS			
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R _{thJA}	-	62	
Case-to-Sink, Flat, Greased Surface	R _{thCS}	0.50	-	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	-	1.0	

PARAMETER	SYMBOL	TEST	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0$	V, I _D = 250 μA	200	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference	to 25 °C, I _D = 1 mA	-	0.29	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V$	/ _{GS} , I _D = 250 μA	2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	VG	_{as} = ± 20 V	-	-	± 100	nA
		V _{DS} = 200 V, V _{GS} = 0 V		-	-	25	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 160 V, V	V _{GS} = 0 V, T _J = 125 °C	-	-	250	μA
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 11 A ^b	-	-	0.18	Ω
Forward Transconductance	9 _{fs}	$V_{DS} = 5$	50 V, I _D = 11 A ^b	6.7	-	-	S
Dynamic						•	
Input Capacitance	C _{iss}	$V_{GS} = 0 V$,		-	1300	-	pF
Output Capacitance	C _{oss}	V	$V_{\rm DS} = 0.0$, $V_{\rm DS} = 25 \text{ V}$, $V_{\rm DS} = 25 \text{ V}$, $V_{\rm DS} = 1.0 \text{ MHz}$, see fig. 5		430	-	
Reverse Transfer Capacitance	C _{rss}	f = 1.0			130	-	
Total Gate Charge	Qg		I _D = 18 A, V _{DS} =160 V, see fig. 6 and 13 ^b	-	-	70	nC
Gate-Source Charge	Q _{gs}	V _{GS} = 10 V		-	-	13	
Gate-Drain Charge	Q _{gd}		see lig. 6 and 13 °		-	39	1
Turn-On Delay Time	t _{d(on)}				14	-	ns
Rise Time	t _r	V_{DD} = 100 V, I_{D} = 18 A, R_{g} = 9.1 Ω , R_{D} = 5.4 Ω , see fig. 10 b		-	51	-	
Turn-Off Delay Time	t _{d(off)}			-	45	-	
Fall Time	t _f			-	36	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from		-	4.5	-	الم
Internal Source Inductance	L _S	package and center of die contact		-	7.5	-	- nH
Gate Input Resistance	Rg	f = 1 MHz, open drain		0.5	-	3.6	Ω
Drain-Source Body Diode Characteristic	s						
Continuous Source-Drain Diode Current	I _S	showing the	MOSFET symbol showing the		-	18	_
Pulsed Diode Forward Current ^a	I _{SM}	integral reverse p - n junction diode		-	-	72	A
Body Diode Voltage	V _{SD}	T _J = 25 °C, I	$T_J = 25 ^{\circ}\text{C}, I_S = 18 \text{A}, V_{GS} = 0 \text{V} ^{\text{b}}$		-	2.0	V
Body Diode Reverse Recovery Time	t _{rr}	T 05 °C 1	10 A dI/d+ 100 A/ h	-	300	610	ns
Body Diode Reverse Recovery Charge	Q _{rr}	$T_J = 25 ^{\circ}\text{C}, I_F = 18 \text{A}, dI/dt = 100 \text{A/}\mu\text{s}^{ \text{b}}$		-	3.4	7.1	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S an				v Ls and	LD)

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300~\mu s;$ duty cycle $\leq 2~\%.$



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

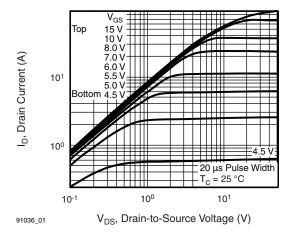


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

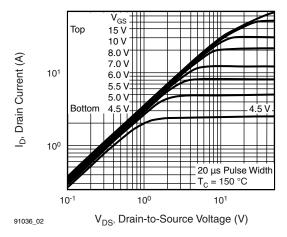


Fig. 2 - Typical Output Characteristics, T_C = 150 °C

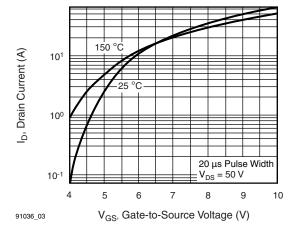


Fig. 3 - Typical Transfer Characteristics

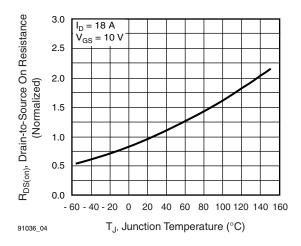


Fig. 4 - Normalized On-Resistance vs. Temperature

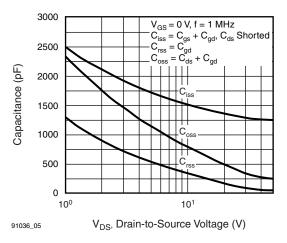


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

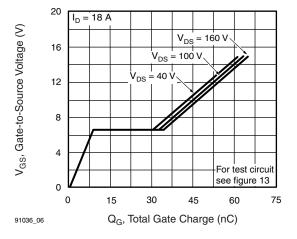


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



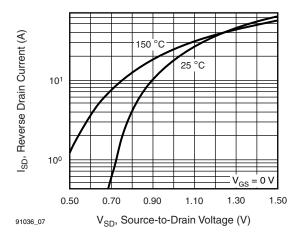


Fig. 7 - Typical Source-Drain Diode Forward Voltage

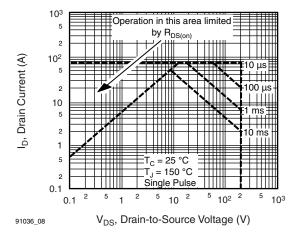


Fig. 8 - Maximum Safe Operating Area

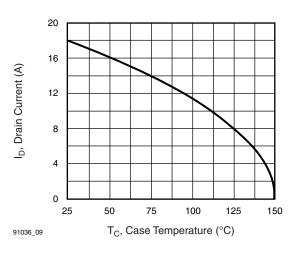


Fig. 9 - Maximum Drain Current vs. Case Temperature

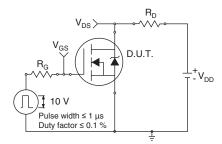


Fig. 10a - Switching Time Test Circuit

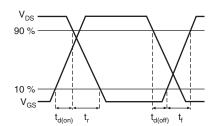


Fig. 10b - Switching Time Waveforms

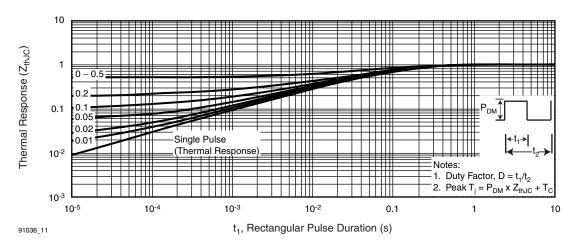


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



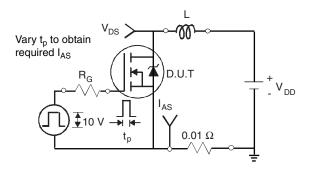


Fig. 12a - Unclamped Inductive Test Circuit

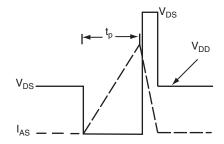


Fig. 12b - Unclamped Inductive Waveforms

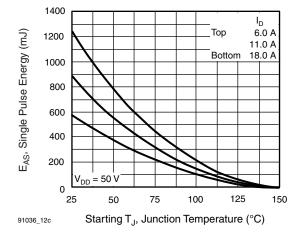


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

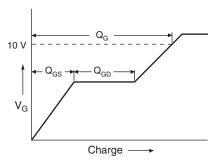


Fig. 13a - Basic Gate Charge Waveform

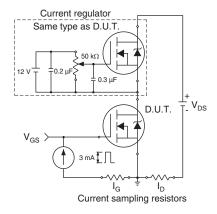
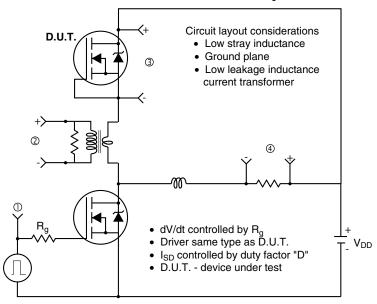
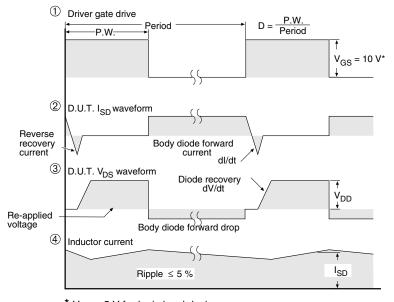


Fig. 13b - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit





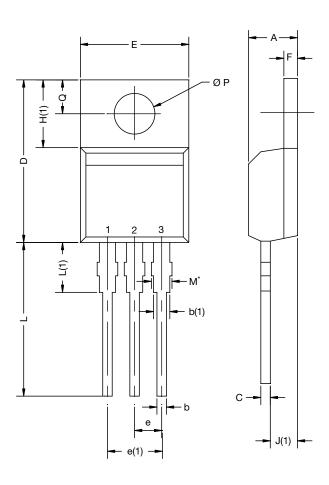
* $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

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TO-220-1



DIM.	MILLIM	METERS	INCHES	
	MIN.	MAX.	MIN.	MAX.
Α	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
С	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
е	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
ØP	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118

Note

DWG: 6031

• $M^* = 0.052$ inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM



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