CD40160BMS, CD40161BMS, CD40162BMS, CD40163BMS

December 1992 File Number 3358

CMOS Synchronous Programmable 4-Bit Counters

CD40160BMS, CD40161BMS, CD40162BMS and CD40163BMS are 4-bit synchronous programmable counters. The CLEAR function of the CD40162BMS and CD40163BMS is synchronous and a low level at the $\overline{\text{CLEAR}}$ input sets all four outputs low on the next positive CLOCK edge. The CLEAR function of the CD40160BMS and CD40161BMS is asychronous and a low level at the $\overline{\text{CLEAR}}$ input sets all four outputs low regardless of the state of the CLOCK, $\overline{\text{LOAD}}$, or ENABLE inputs. A low level at the $\overline{\text{LOAD}}$ input disables the counter and causes the output to agree with the setup data after the next CLOCK pulse regardless of the conditions of the ENABLE inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output (COUT). Counting is enabled when both PE and TE inputs are high. The TE input is fed forward to enable COUT. This enabled output produces a positive output pulses with a duration approximately equal to the positive portion of the Q1 output. This positive overflow carry pulse can be used to enable successive cascaded stages. Logic transitions at the PE or TE inputs may occur when the clock is either high or low.

The CD40160BMS through CD40163BMS types are functionally equivalent to and pin-compatible with the TTL counter series 74LS160 through 74LS163 respectively.

The CD40160BMS, CD40161BMS, CD40162BMS and CD40163BMS are supplied in these 16 lead outline packages:

	CD40160	CD40161	CD40162	CD40163
Braze Seal DIP	H4W	H4X	H4X	H4W
Frit Seal DIP	H1F	H1F	H1L	H1F
Ceramic Flatpack	H6P	H6W	H6P	H6W

Features

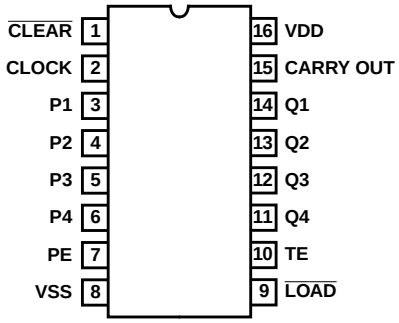
- **High-Voltage Types (20V Rating)**
- **CD40160BMS Decade with Asynchronous Clear**
- **CD40161BMS Binary with Asynchronous Clear**
- **CD40162BMS Decade with Synchronous Clear**
- **CD40163BMS Binary with Synchronous Clear**
- **Internal Look-Ahead for Fast Counting**
- **Carry Output for Cascading**
- **Synchronously Programmable**
- **Clear Asynchronous Input (CD40160BMS, CD40161BMS)**
- **Clear Synchronous Input (CD40162BMS, CD40163BMS)**
- **Synchronous Load Control Input**
- **Low Power TTL Compatibility**
- **Standardized Symmetrical Output Characteristics**
- **100% Tested for Quiescent Current at 20V**
- **Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C**
- **Noise Margin (Over Full Package Temperature Range):**
  - **1V at VDD = 5V**
  - **2V at VDD = 10V**
  - **2.5V at VDD = 15V**
- **5V, 10V and 15V Parametric Ratings**
- **Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications

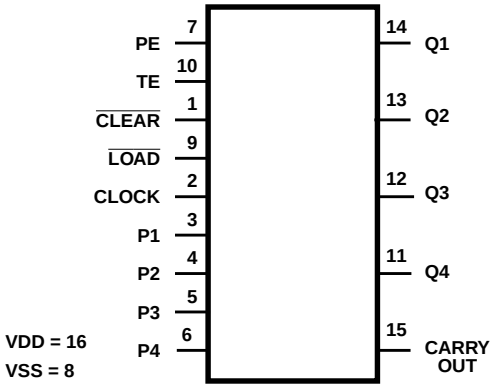
- **Programmable Binary and Decade Counting**
- **Counter Control/Timers**
- **Frequency Dividing**

Pinout

CD40160BMS, CD40161BMS, CD40162BMS, CD40163BMS
TOP VIEW



Functional Diagram



Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) . . . . . -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs . . . . . -0.5V to VDD +0.5V
DC Input Current, Any One Input. . . . . ±10mA
Operating Temperature Range . . . . . -55^oC to $+125^oC$
Package Types D, F, K, H
Storage Temperature Range (TSTG). . . . . -65^oC to $+150^oC$
Lead Temperature (During Soldering) . . . . . $+265^oC$
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	$80^oC/W$	$20^oC/W$
Flatpack Package	$70^oC/W$	$20^oC/W$

Maximum Package Power Dissipation (PD) at $+125^oC$
For T_A = -55^oC to $+100^oC$ (Package Type D, F, K). 500mW
For T_A = $+100^oC$ to $+125^oC$ (Package Type D, F, K) . . . . . Derate Linearity at 12mW/^oC to 200mW
Device Dissipation per Output Transistor. 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature . . . . . $+175^oC$

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	$+25^oC$	-	10	µA
				2	$+125^oC$	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55^oC	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	$+25^oC$	-100	-	nA
				2	$+125^oC$	-1000	-	nA
			VDD = 18V	3	-55^oC	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	$+25^oC$	-	100	nA
				2	$+125^oC$	-	1000	nA
			VDD = 18V	3	-55^oC	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	$+25^oC$	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	$+25^oC$	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	$+25^oC$	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	$+25^oC$	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	$+25^oC$	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	$+25^oC$	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	$+25^oC$	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	$+25^oC$	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	$+25^oC$	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	$+25^oC$	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	$+25^oC$			
		VDD = 18V, VIN = VDD or GND		8A	$+125^oC$			
		VDD = 3V, VIN = VDD or GND		8B	-55^oC			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	11	-	V

NOTES:
1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock to Q	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Propagation Delay Clock to COut	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	450	ns
			10, 11	+125°C, -55°C	-	608	ns
Propagation Delay TE to COut	TPHL3 TPLH3	VDD = 5V, VIN = VDD or GND	9	+25°C	-	250	ns
			10, 11	+125°C, -55°C	-	338	ns
Propagation Delay CD40160BMS, CD40161BMS $\overline{\text{Clear}}$ to Q	TPHL4	VDD = 5V, VIN = VDD or GND	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	675	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	2	-	MHz
			10, 11	+125°C, -55°C	1.48	-	MHz

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125^{O}C	-	-2.4	mA
				-55^{O}C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25^{O}C, +125^{O}C, -55^{O}C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25^{O}C, +125^{O}C, -55^{O}C	7	-	V
Propagation Delay Clock to Q	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25^{O}C	-	160	ns
		VDD = 15V	1, 2, 3	+25^{O}C	-	120	ns
Propagation Delay Clock to C Out	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25^{O}C	-	190	ns
		VDD = 15V	1, 2, 3	+25^{O}C	-	140	ns
Propagation Delay TE to C Out	TPHL3 TPLH3	VDD = 10V	1, 2, 3	+25^{O}C	-	110	ns
		VDD = 15V	1, 2, 3	+25^{O}C	-	80	ns
Propagation Delay CD40160BMS, CD40161BMS Clear to Q	TPHL4	VDD = 10V	1, 2, 3	+25^{O}C	-	220	ns
		VDD = 15V	1, 2, 3	+25^{O}C	-	160	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25^{O}C	-	100	ns
		VDD = 15V	1, 2, 3	+25^{O}C	-	80	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2, 3	+25^{O}C	5.5	-	MHz
		VDD = 15V	1, 2, 3	+25^{O}C	8	-	MHz
Maximum Clock Rise or Fall Time	TRCL TFCL	VDD = 5V	1, 2, 3, 4	+25^{O}C	-	200	µs
		VDD = 10V	1, 2, 3, 4	+25^{O}C	-	70	µs
		VDD = 15V	1, 2, 3, 4	+25^{O}C	-	15	µs
Minimum Data Hold Time Clock Operation	TH	VDD = 5V	1, 2, 3	+25^{O}C	-	0	ns
		VDD = 10V	1, 2, 3	+25^{O}C	-	0	ns
		VDD = 15V	1, 2, 3	+25^{O}C	-	0	ns
Minimum Clock Pulse Width Clock Operation	TW	VDD = 5V	1, 2, 3	+25^{O}C	-	170	ns
		VDD = 10V	1, 2, 3	+25^{O}C	-	70	ns
		VDD = 15V	1, 2, 3	+25^{O}C	-	50	ns
Minimum Setup Time Data to Clock	TS	VDD = 5V	1, 2, 3	+25^{O}C	-	240	ns
		VDD = 10V	1, 2, 3	+25^{O}C	-	90	ns
		VDD = 15V	1, 2, 3	+25^{O}C	-	60	ns
Minimum Setup Time $\overline{\text{Load}}$ to Clock	TS	VDD = 5V	1, 2, 3	+25^{O}C	-	240	ns
		VDD = 10V	1, 2, 3	+25^{O}C	-	90	ns
		VDD = 15V	1, 2, 3	+25^{O}C	-	60	ns
Minimum Setup Time PE to TE to Clock	TS	VDD = 5V	1, 2, 3	+25^{O}C	-	340	ns
		VDD = 10V	1, 2, 3	+25^{O}C	-	140	ns
		VDD = 15V	1, 2, 3	+25^{O}C	-	100	ns
Minimum $\overline{\text{Clear}}$ Pulse Width (CD40160BMS, CD40161BMS)	TW	VDD = 5V	1, 2, 3	+25^{O}C	-	170	ns
		VDD = 10V	1, 2, 3	+25^{O}C	-	70	ns
		VDD = 15V	1, 2, 3	+25^{O}C	-	50	ns
Minimum Setup Time $\overline{\text{Clear}}$ to Clock (CD40162BMS, CD40163BMS)	TS	VDD = 5V	1, 2, 3	+25^{O}C	-	340	ns
		VDD = 10V	1, 2, 3	+25^{O}C	-	140	ns
		VDD = 15V	1, 2, 3	+25^{O}C	-	100	ns
Minimum Hold Time $\overline{\text{Clear}}$ to Clock (CD40162BMS, CD40163BMS)	TH	VDD = 5V	1, 2, 3	+25^{O}C	-	0	ns
		VDD = 10V	1, 2, 3	+25^{O}C	-	0	ns
		VDD = 15V	1, 2, 3	+25^{O}C	-	0	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Minimum $\overline{\text{Clear}}$ Removal Time (CD40160BMS, CD40161BMS)	TREM	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	70	ns

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. If more than one unit is cascaded, TRCL should be made less than or equal to the sumof the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	11 - 15	1 - 10	16			
Static Burn-In 2 Note 1	11 - 15	8	1 - 7, 9, 10, 16			
Dynamic Burn-In Note 1	-	8	1, 7, 9, 10, 16	11 - 15	2 - 6	-
Irradiation Note 2	11 - 15	8	1 - 7, 9, 10, 16			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagrams

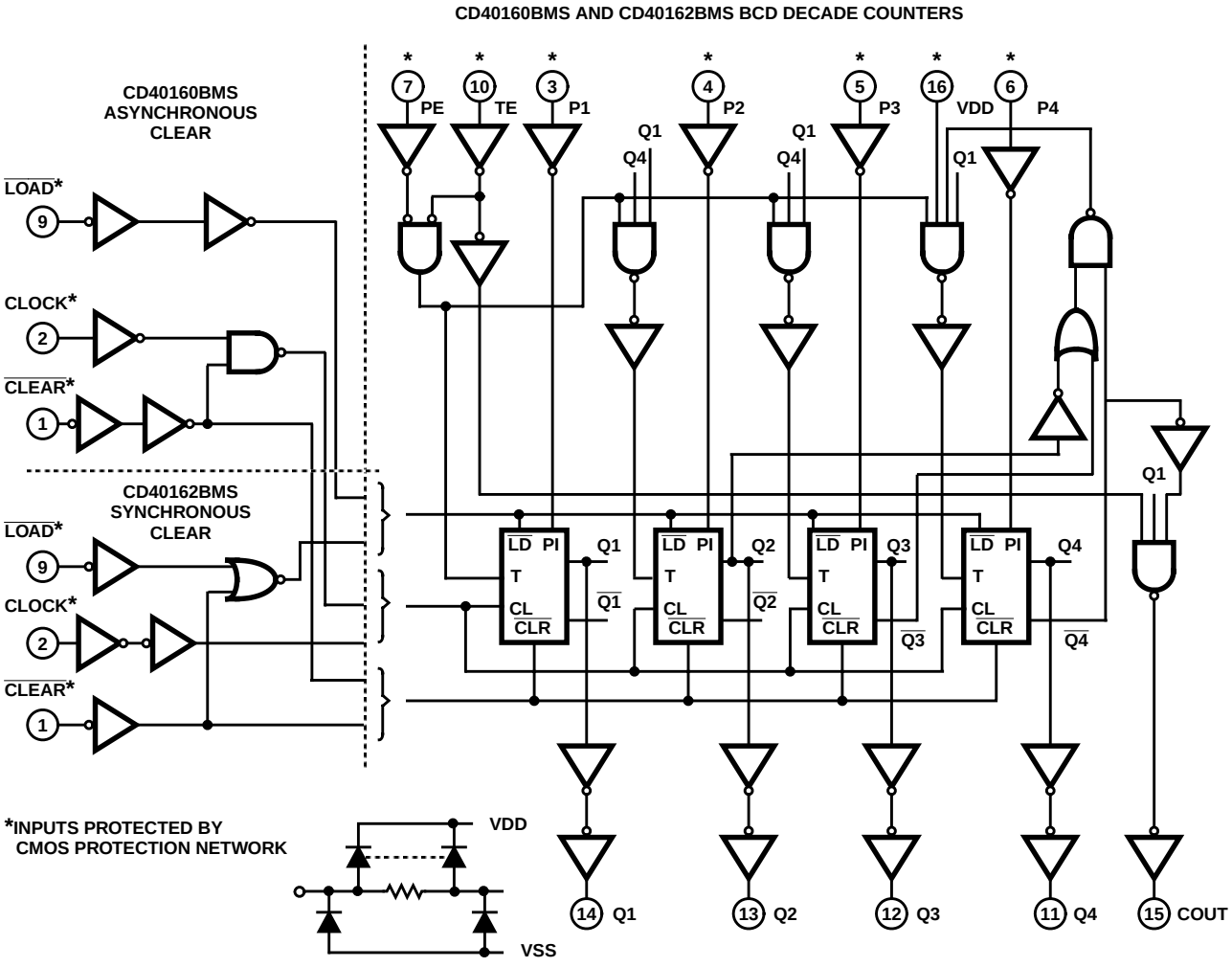


FIGURE 1. LOGIC DIAGRAM FOR CD40160BMS AND CD40162BMS BCD DECADE COUNTERS

Logic Diagrams (Continued)

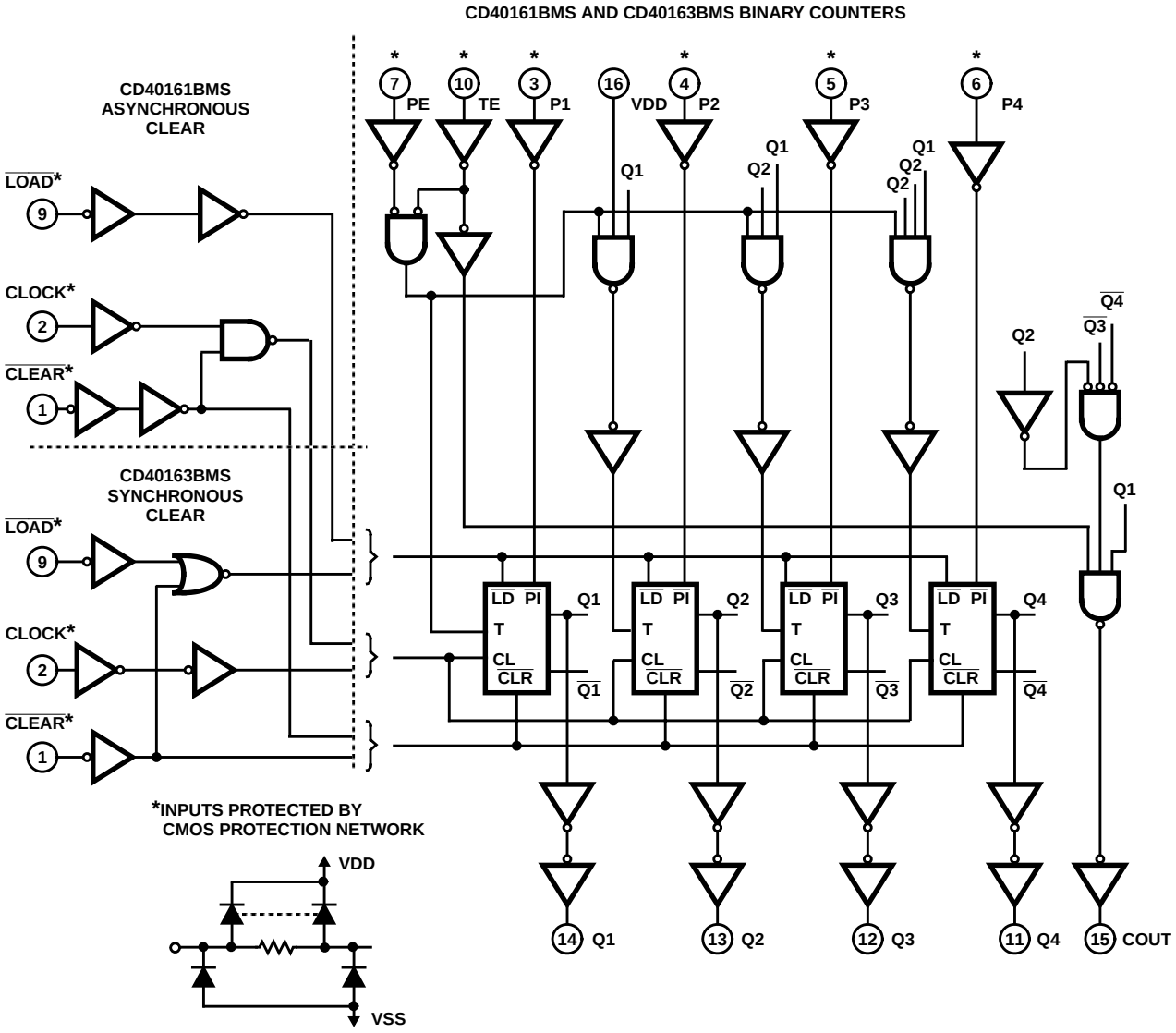


FIGURE 2. LOGIC DIAGRAM FOR CD40161BMS AND CD40163BMS BINARY COUNTERS

TRUTH TABLE

CLOCK	$\overline{CLR}$	$\overline{LOAD}$	PE	TE	OPERATION
⎍	1	0	X	X	Preset
⎍	1	1	0	X	NC
⎍	1	1	X	0	NC
⎍	1	1	1	1	Count
X	0	X	X	X	Reset (CD40160BMS, CD40161BMS)
⎍	0	X	X	X	Reset (CD40162BMS, CD40163BMS)
⎎	1	X	X	X	NC (CD40162BMS, CD40163BMS)

1 = High Level
0 = Low Level
X = Don't Care
NC = No Change

Typical Performance Characteristics

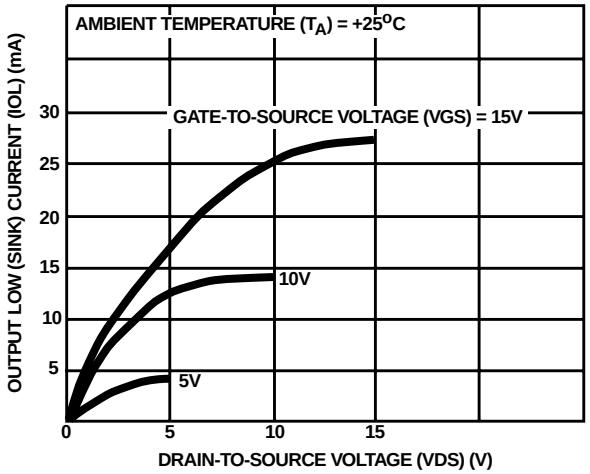


FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

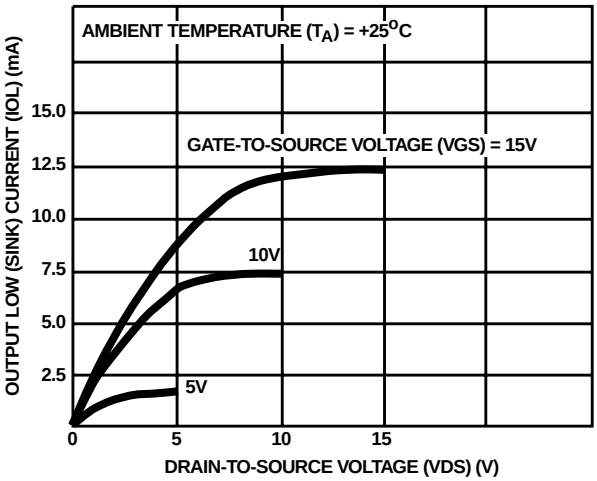


FIGURE 4. MIMIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

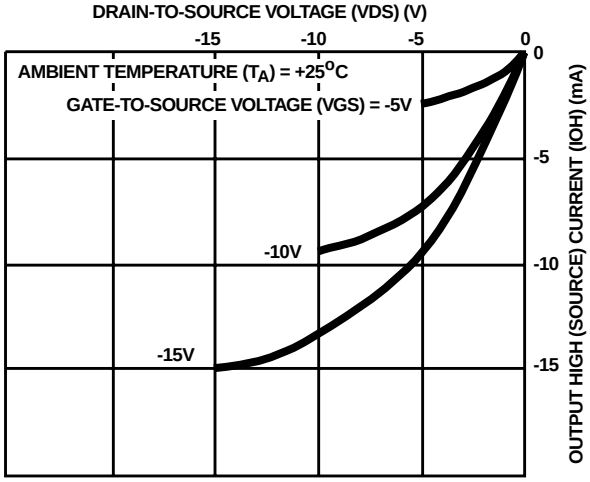


FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

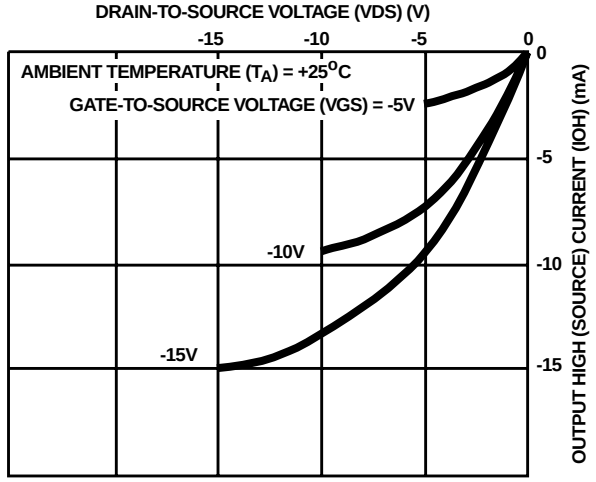


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

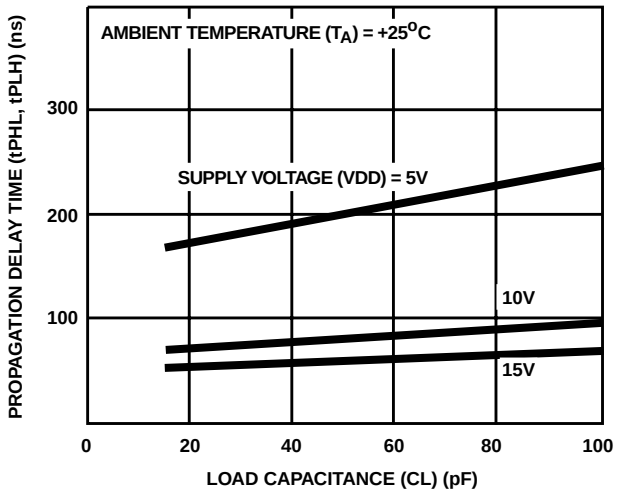


FIGURE 7. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (CLOCK TO Q)

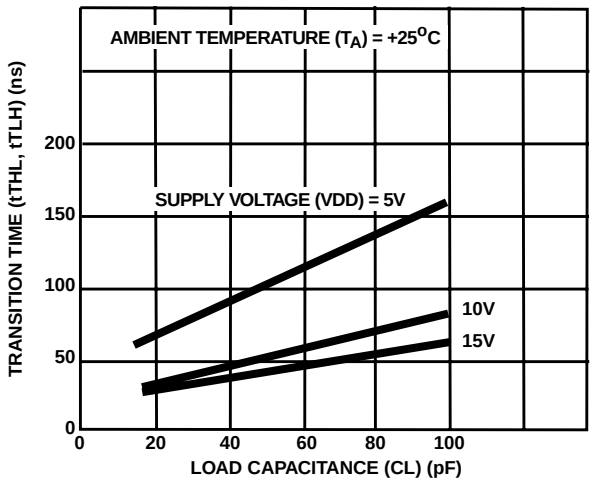


FIGURE 8. TYPICAL TRANSISTION TIME AS A FUNCTION OF LOAD CAPACITANCE

Typical Performance Characteristics (Continued)

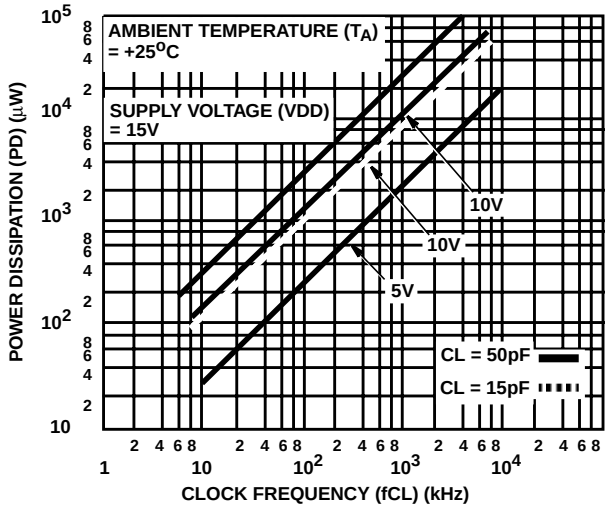


FIGURE 9. TYPICAL POWER DISSIPATION AS A FUNCTION OF CLOCK FREQUENCY

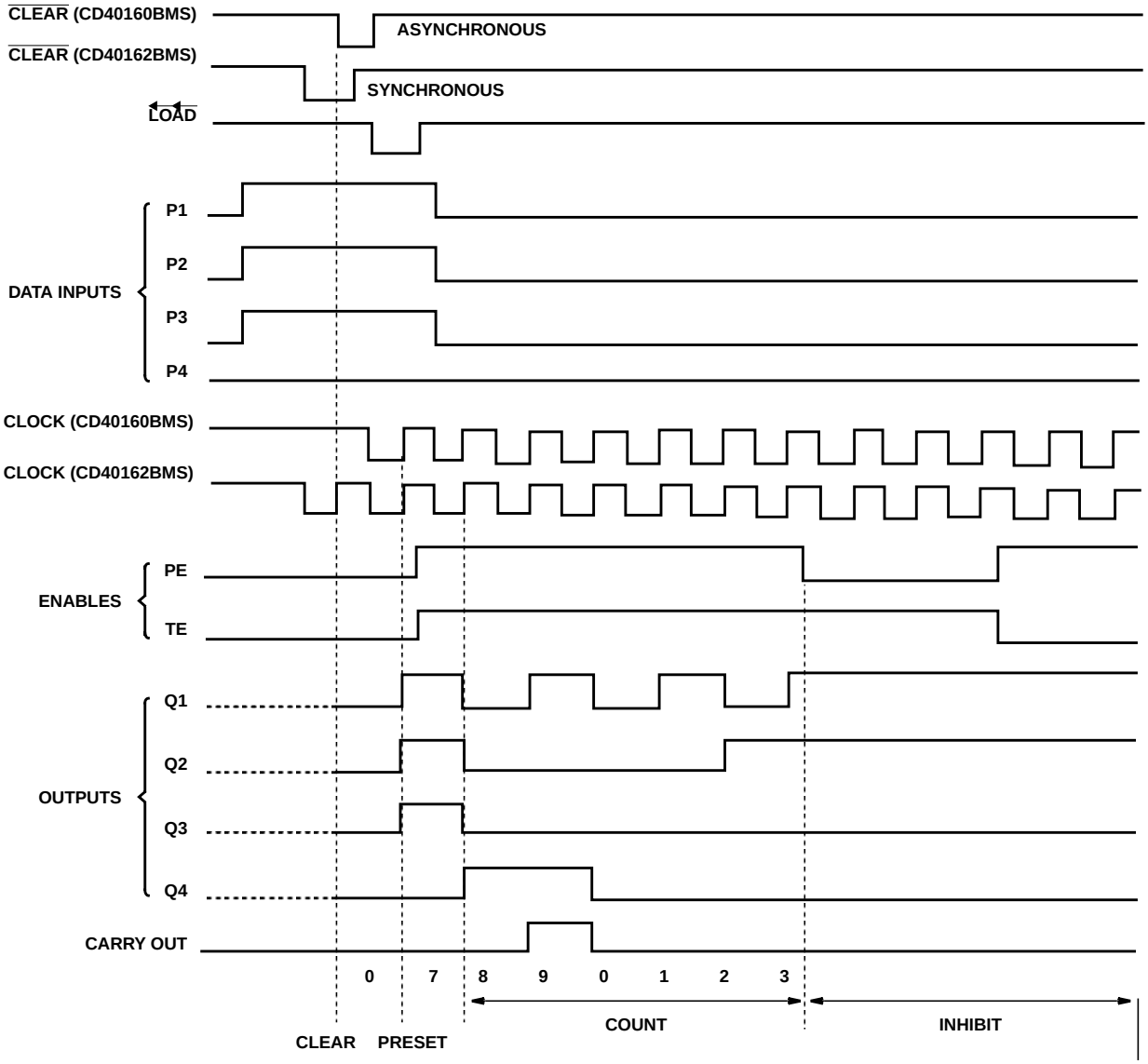


FIGURE 10. TIMING DIAGRAM FOR CD40160BMS, CD40162BMS

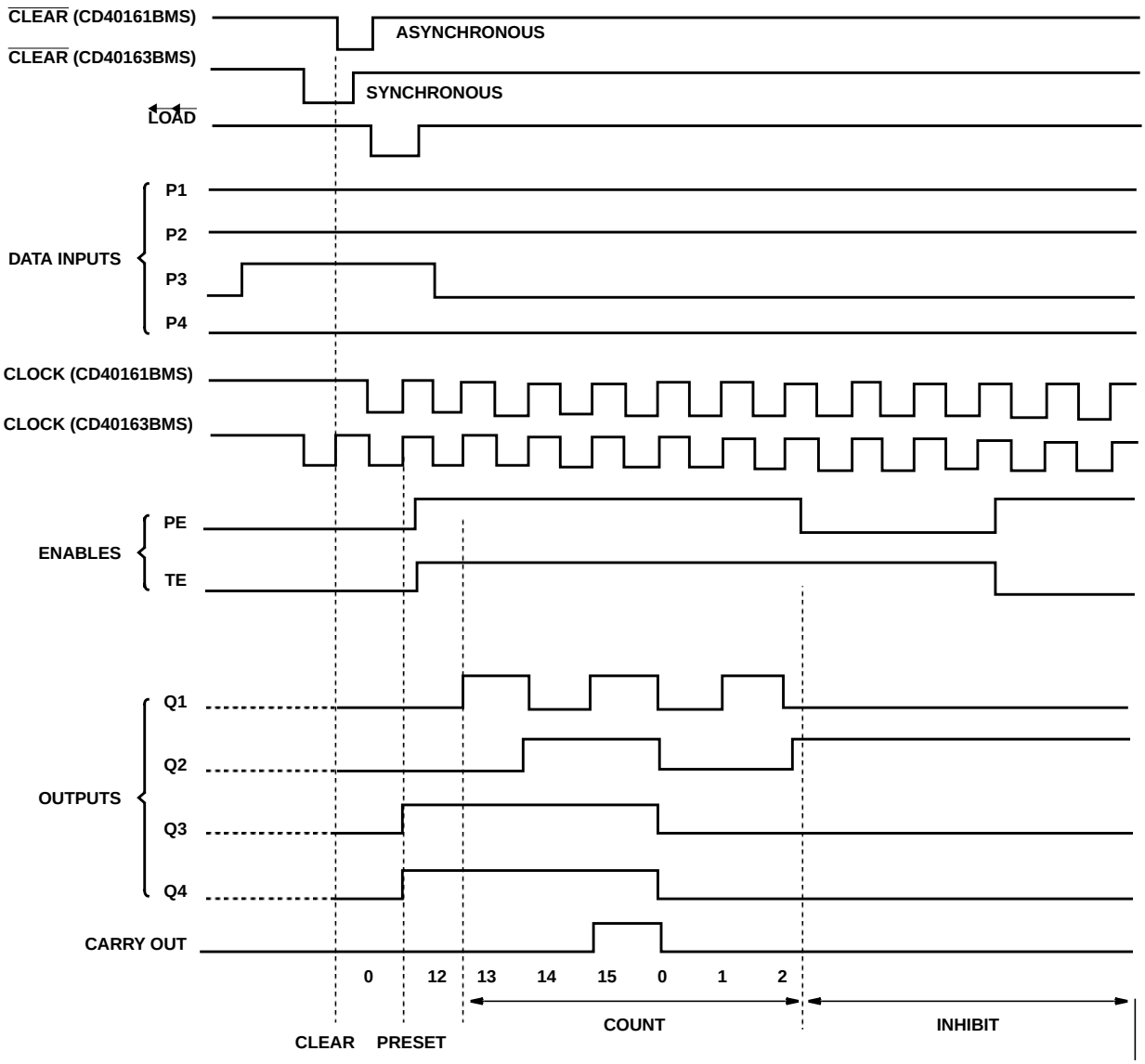


FIGURE 11. TIMING DIAGRAM FOR CD40161BMS AND CD40163BMS

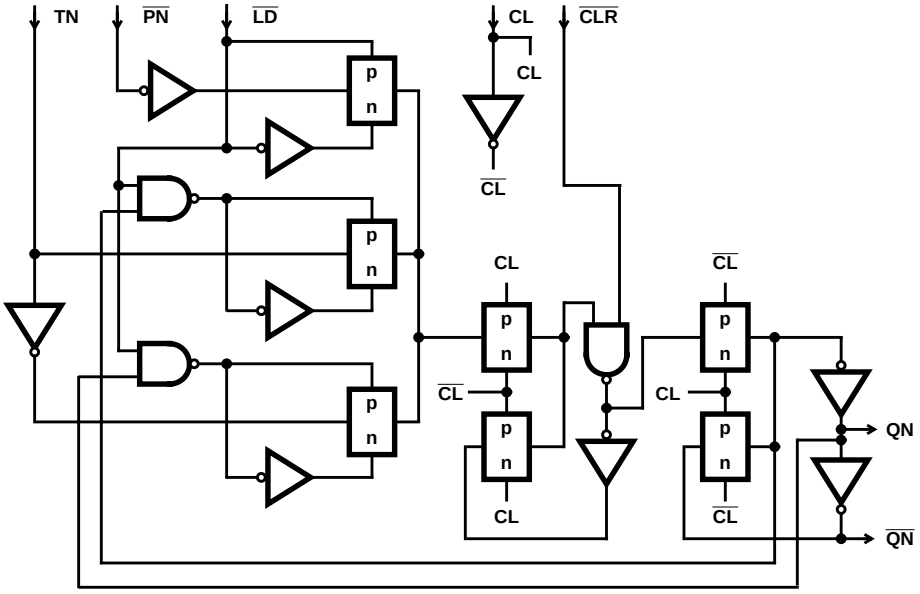


FIGURE 12. DETAIL OF FLIP-FLOPS OF CD40160BMS AND CD40161BMS (ASYNCHRONOUS CLEAR)

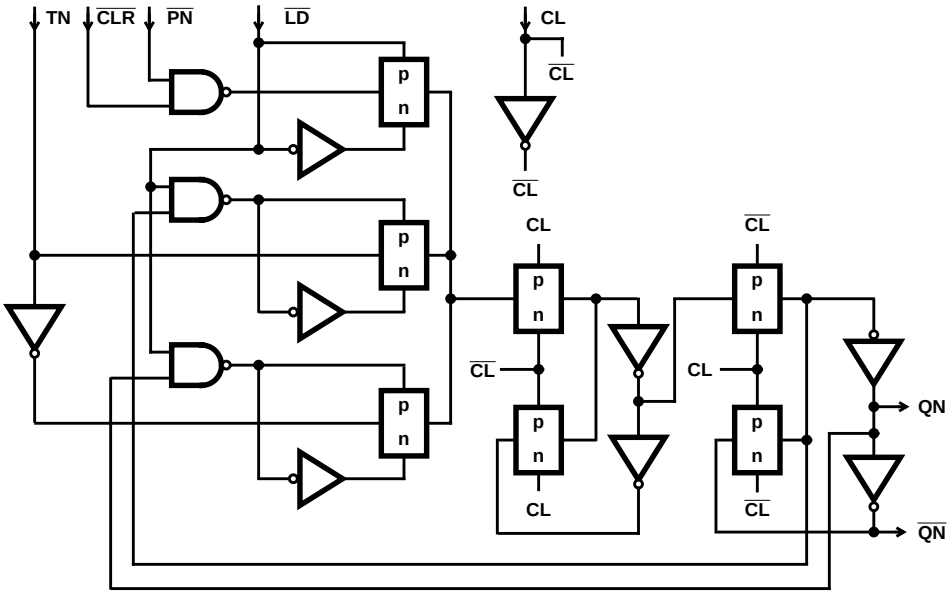


FIGURE 13. DETAIL OF FLIP-FLOPS OF CD40162BMS AND CD40163BMS (SYNCHRONOUS CLEAR)

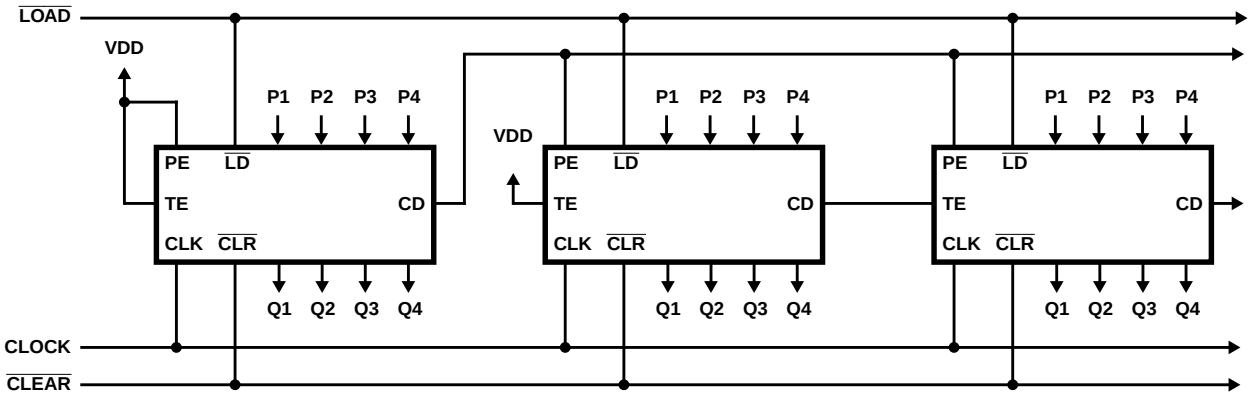


FIGURE 14. CASCADED COUNTER PACKAGES IN THE PARALLEL-CLOCKED MODE

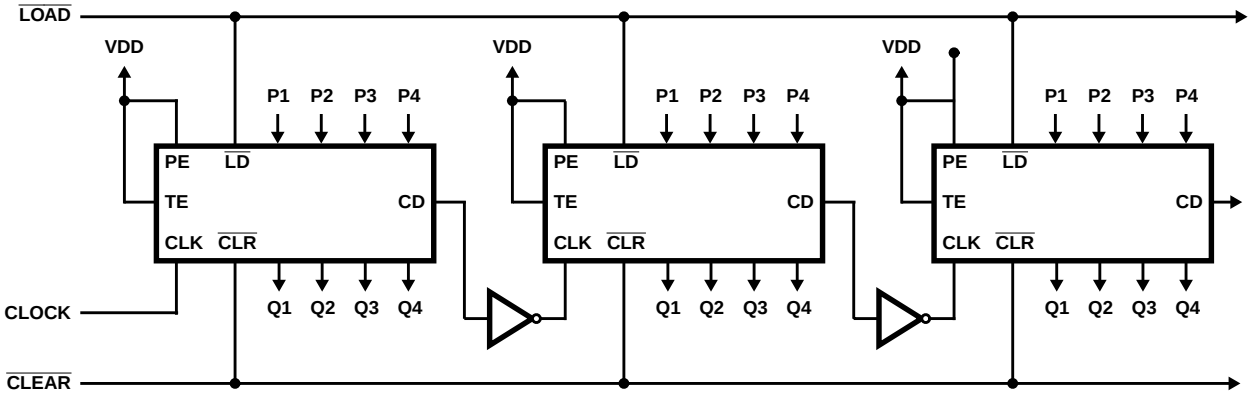
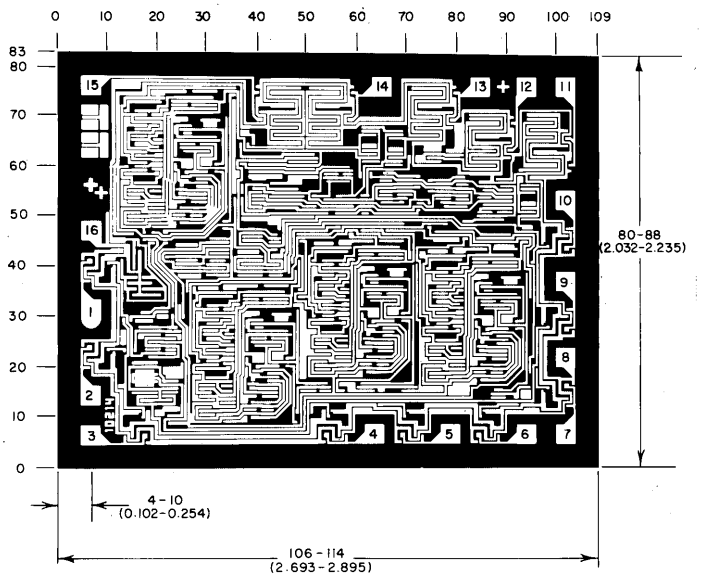


FIGURE 15. CASCADED COUNTER PACKAGES IN THE RIPPLE-CLOCKED MODE

Chip Dimensions and Pad Layout



Dimensions and pad layout for CD40160BMSH. Dimensions and pad layout for CD40161BMS, CD40162BMSH, and CD40163BMSH are identical.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.
PASSIVATION: 10.4kÅ - 15.6kÅ, Silane
BOND PADS: 0.004 inches X 0.004 inches MIN
DIE THICKNESS: 0.0198 inches - 0.0218 inches

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