SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A, SN54S162, SN54S163, SN74160 THRU SN74163, SN74LS160A THRU SN74LS163A, SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS
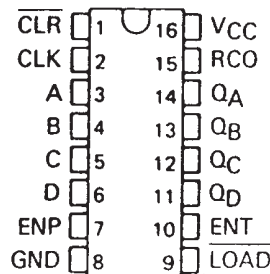
SDLS060 – OCTOBER 1976 – REVISED MARCH 1988

'160,'161,'LS160A,'LS161A . . . SYNCHRONOUS COUNTERS WITH DIRECT CLEAR
'162,'163,'LS162A,'LS163A,'S162,'S163 . . . FULLY SYNCHRONOUS COUNTERS

- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Load Control Line
- Diode-Clamped Inputs

TYPE	TYPICAL PROPAGATION TIME, CLOCK TO Q OUTPUT	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'160 thru '163	14 ns	32 MHz	305 mW
'LS162A thru 'LS163A	14 ns	32 MHz	93 mW
'S162 and 'S163	9 ns	70 MHz	475 mW

SERIES 54', 54LS' 54S' . . . J OR W PACKAGE
SERIES 74' . . . N PACKAGE
SERIES 74LS', 74S' . . . D OR N PACKAGE
(TOP VIEW)

```
        ___  ____
CLR [ 1  U  16 ] VCC
CLK [ 2     15 ] RCO
  A [ 3     14 ] QA
  B [ 4     13 ] QB
  C [ 5     12 ] QC
  D [ 6     11 ] QD
ENP [ 7     10 ] ENT
GND [ 8      9 ] LOAD
```
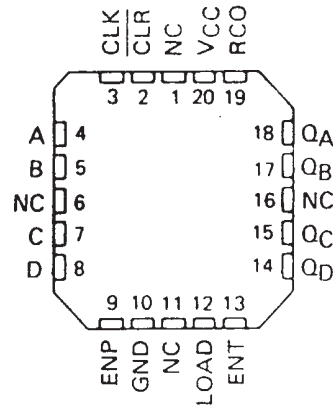
NC—No internal connection

SERIES 54LS', 54S' . . . FK PACKAGE
(TOP VIEW)

```
        CLK CLR NC VCC RCO
         3   2  1  20  19
   A [ 4            18 ] QA
   B [ 5            17 ] QB
  NC [ 6            16 ] NC
   C [ 7            15 ] QC
   D [ 8            14 ] QD
         9  10 11 12 13
        ENP GND NC LOAD ENT
```

NC—No internal connection

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The '160,'162,'LS160A,'LS162A, and 'S162 are decade counters and the '161,'163,'LS161A,'LS163A, and 'S163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters, however counting spikes may occur on the (RCO) ripple carry output. A buffered clock input triggers the four flip-flops on the rising edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input of the '160 thru '163 should be avoided when the clock is low if the enable inputs are high at or before the transition. This restriction is not applicable to the 'LS160A thru 'LS163A or 'S162 or 'S163. The clear function for the '160, '161,'LS160A, and 'LS161A is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs. The clear function for the '162,'163,'LS162A,'LS163A, 'S162, and 'S163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL). Low-to-high transitions at the clear input of the '162 and '163 should be avoided when the clock is low if the enable and load inputs are high at or before the transition.

Copyright © 1988, Texas Instruments Incorporated

TEXAS INSTRUMENTS

SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A, SN54S162, SN54S163, SN74160 THRU SN74163, SN74LS160A THRU SN74LS163A, SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

SDLS060 – OCTOBER 1976 – REVISED MARCH 1988

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs of the '160 thru '163 should occur only when the clock input is high. Transitions at the enable P or T inputs of the 'LS160A thru 'LS163A or 'S162 and 'S163 are allowed regardless of the level of the clock input.

'LS160A thru 'LS163A, 'S162 and 'S163 feature a fully independent clock circuit. Changes at control inputs (enable P or T, or load) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

logic symbols[†]

[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

SN54LS160A THRU SN54LS163A, SN54S162,
SN54S163, SN74LS160A THRU SN74LS163A,
SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

SDLS060 – OCTOBER 1976 – REVISED MARCH 1988

logic symbols (continued)†

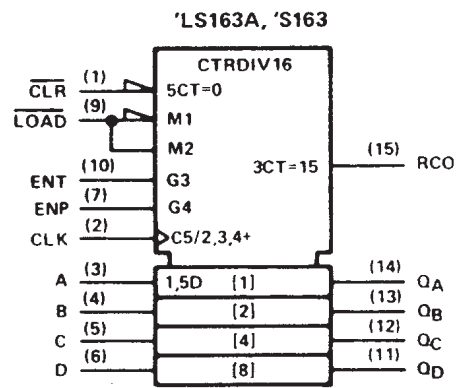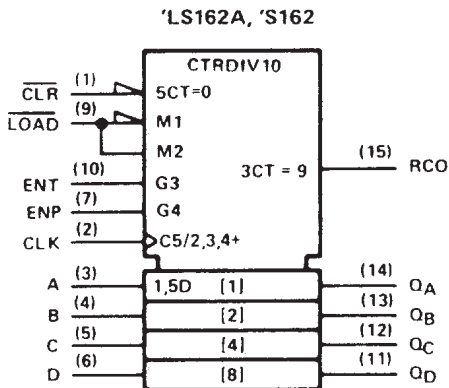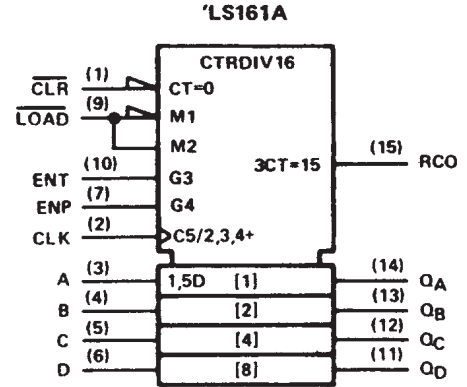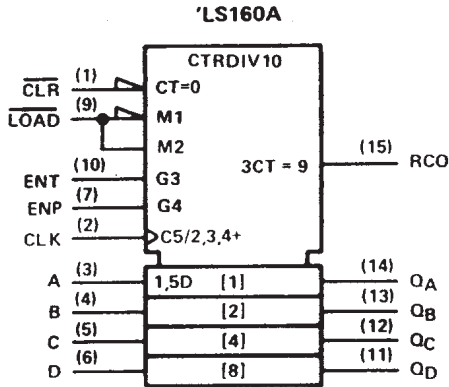'LS160A

'LS161A

'LS162A, 'S162

'LS163A, 'S163

†These symbols are in accordance with ANSI/IEEE Std 91-1984 and
IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)

SN54160, SN74160 SYNCHRONOUS DECADE COUNTERS

SN54162, SN74162 synchronous decade counters are similar; however the clear is synchronous as shown for the SN54163, SN74163 binary counters at right.
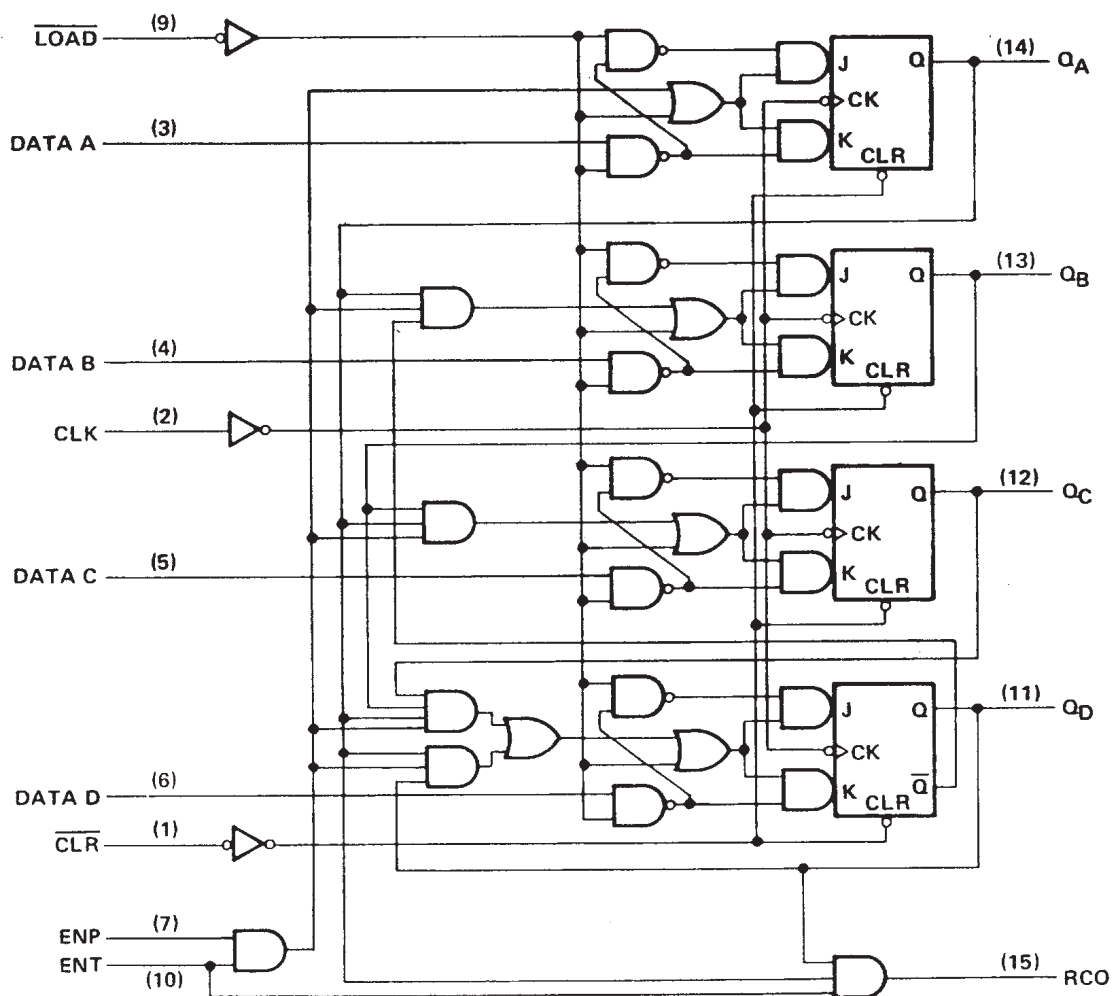
Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)

SN54163, SN74163 SYNCHRONOUS BINARY COUNTERS

SN54161, SN74161 synchronous binary counters are similar; however, the clear is asynchronous as shown for the SN54160, SN74160 decade counters at left.

Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)

SN54LS160A, SN74LS160A SYNCHRONOUS
DECADE COUNTERS

SN54LS162A, SN74LS162A synchronous decade
counters are similar; however the clear is synchronous
as shown for the SN54LS163A, SN74LS163A binary
counters at right.

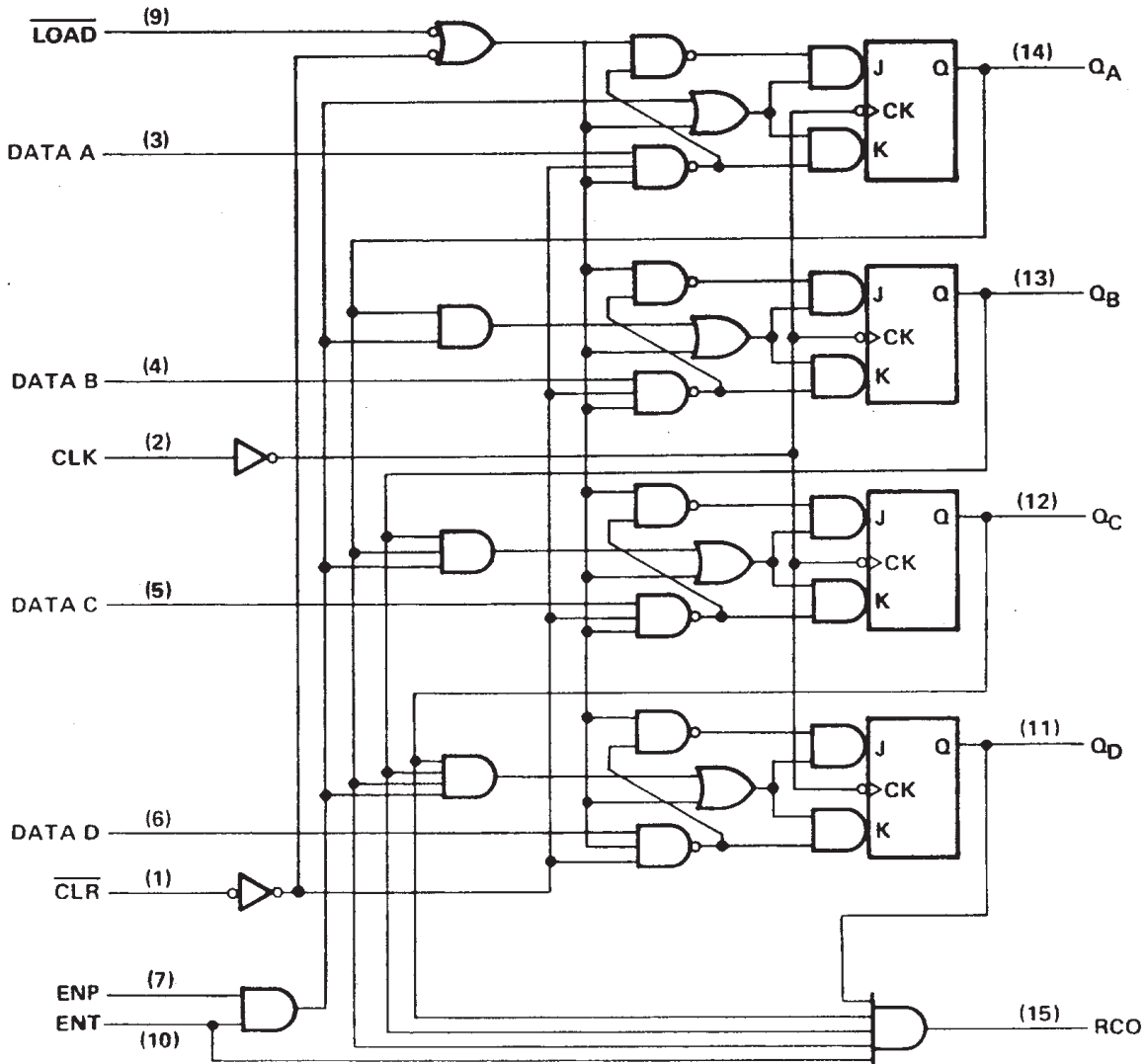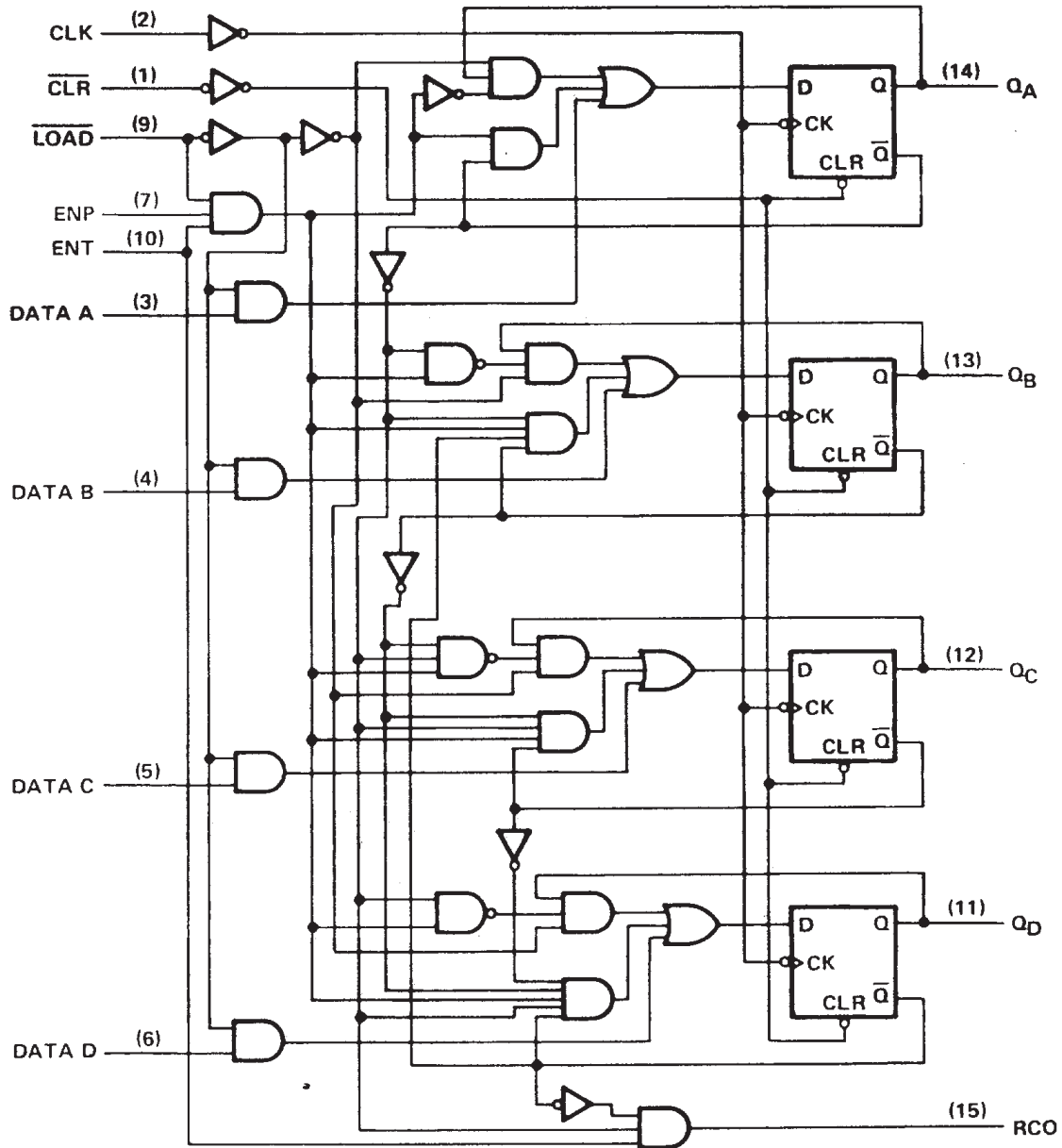Pin numbers shown are for D, J, N, and W packages.

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

logic diagram (positive logic)

SN54LS163A, SN74LS163A SYNCHRONOUS
BINARY COUNTERS

SN54LS161A, SN74LS161A synchronous binary counters are similar; however, the clear is asynchronous as shown for the SN54LS160A, SN74LS160A decade counters at left.
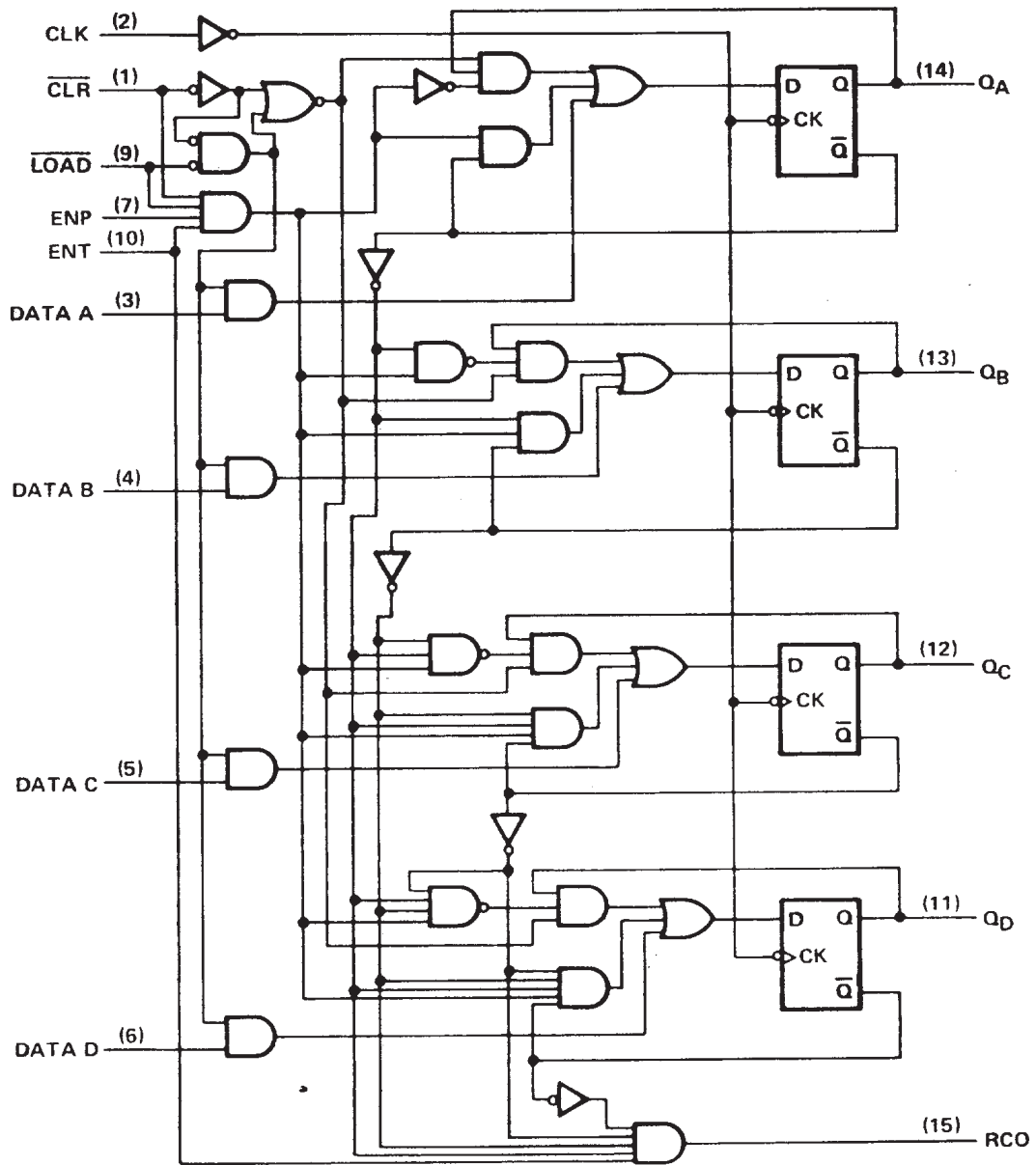
Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)

SN54S162, SN74S162 SYNCHRONOUS DECADE COUNTER

Pin numbers shown are for D, J, N, and W packages.

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

logic diagram (positive logic)

SN54S163, SN74S163 SYNCHRONOUS DECADE COUNTER

Pin numbers shown are for D, J, N, and W packages.

9
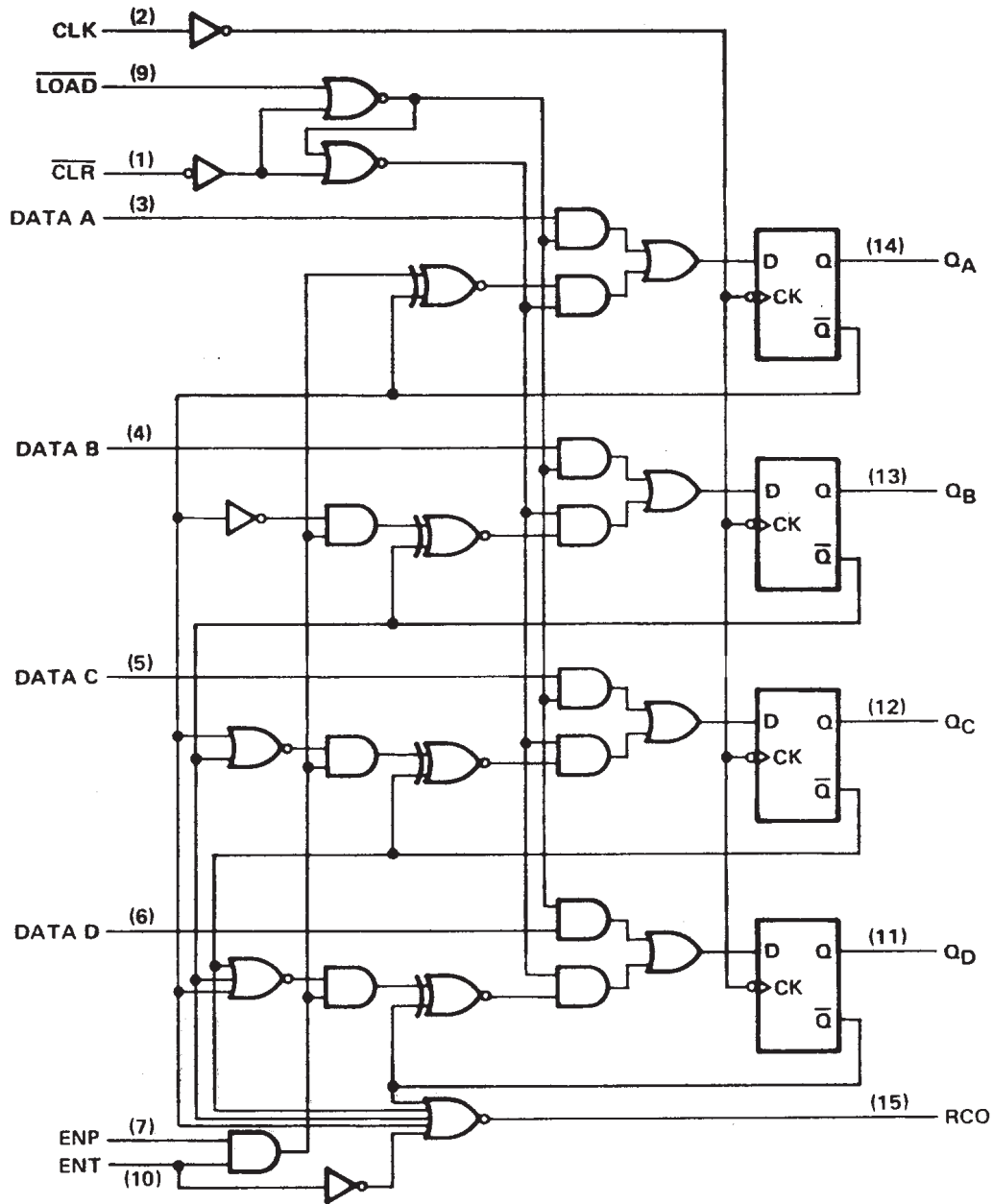
SN54160, SN54162, SN54LS160A, SN54LS162A, SN54S162,
SN74160, SN74162, SN74LS160A, SN74LS162A, SN74S162
SYNCHRONOUS 4-BIT COUNTERS

SDLS060 – OCTOBER 1976 – REVISED MARCH 1988

'160, '162, 'LS160A, 'LS162A, 'S162 DECADE COUNTERS

typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero ('160 and 'LS160A are asynchronous; '162, 'LS162A, and 'S162 are synchronous)
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265
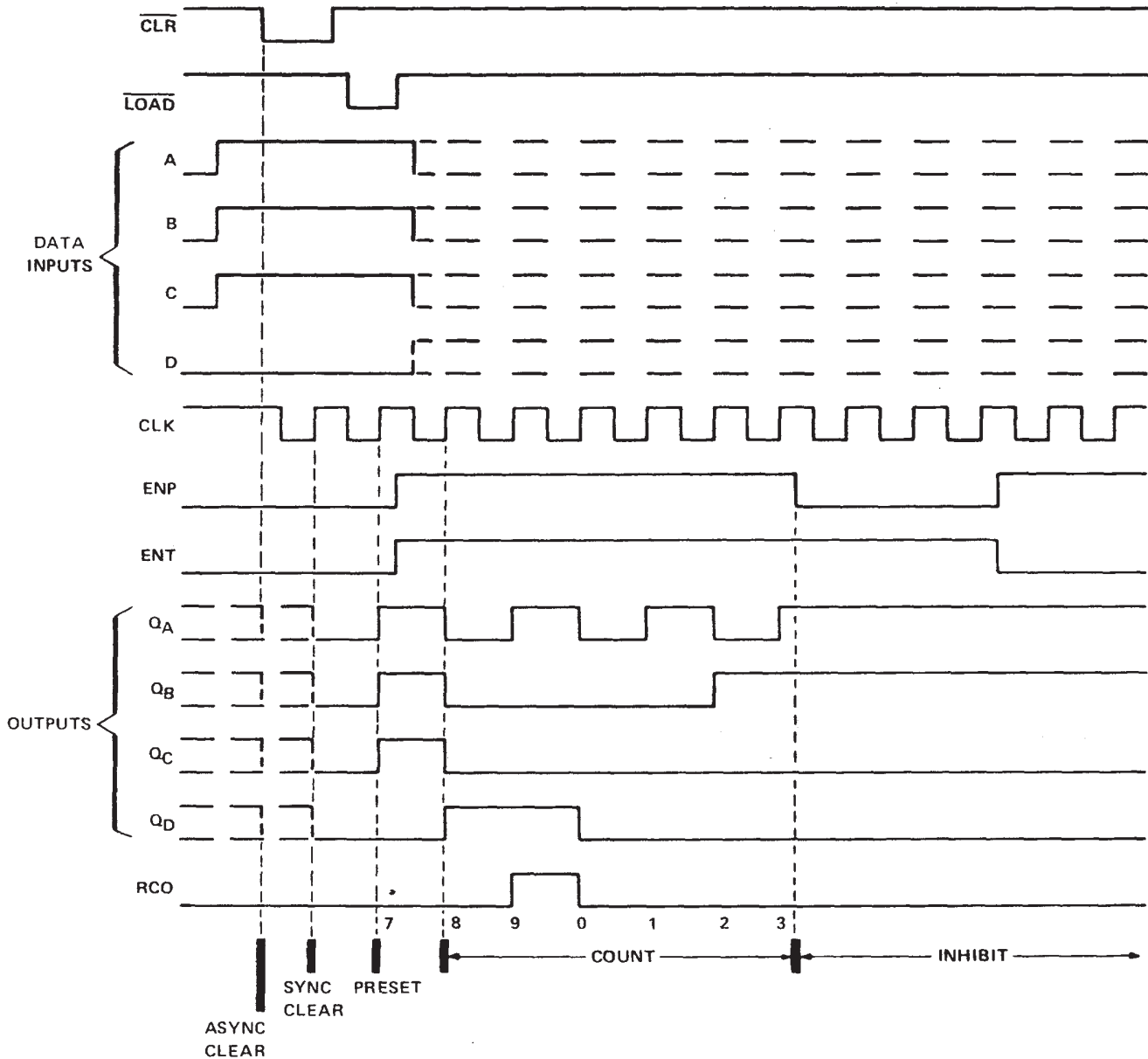
'161, 'LS161A, '163, 'LS163A, 'S163 BINARY COUNTERS

typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:
1. Clear outputs to zero ('161 and 'LS161A are asynchronous; '163, 'LS163A, and 'S163 are synchronous)
2. Preset to binary twelve
3. Count to thirteen, fourteen fifteen, zero, one, and two
4. Inhibit

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

CLK: R_{eq} = 2.8 kΩ NOM
ENT: R_{eq} = 2 kΩ NOM
$\overline{\text{CLR}}$, ENP: R_{eq} = 4 kΩ NOM
A, B, C, D: R_{eq} = 6 kΩ NOM

TYPICAL OF ALL OUTPUTS

130 Ω NOM
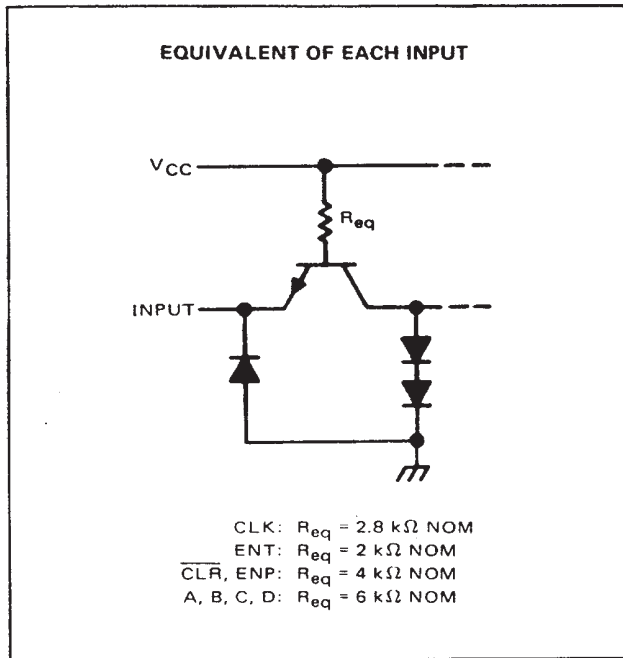
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . 5.5 V
Operating free-air temperature range: SN54' Circuits . . . . −55°C to 125°C
SN74' Circuits . . . . 0°C to 70°C
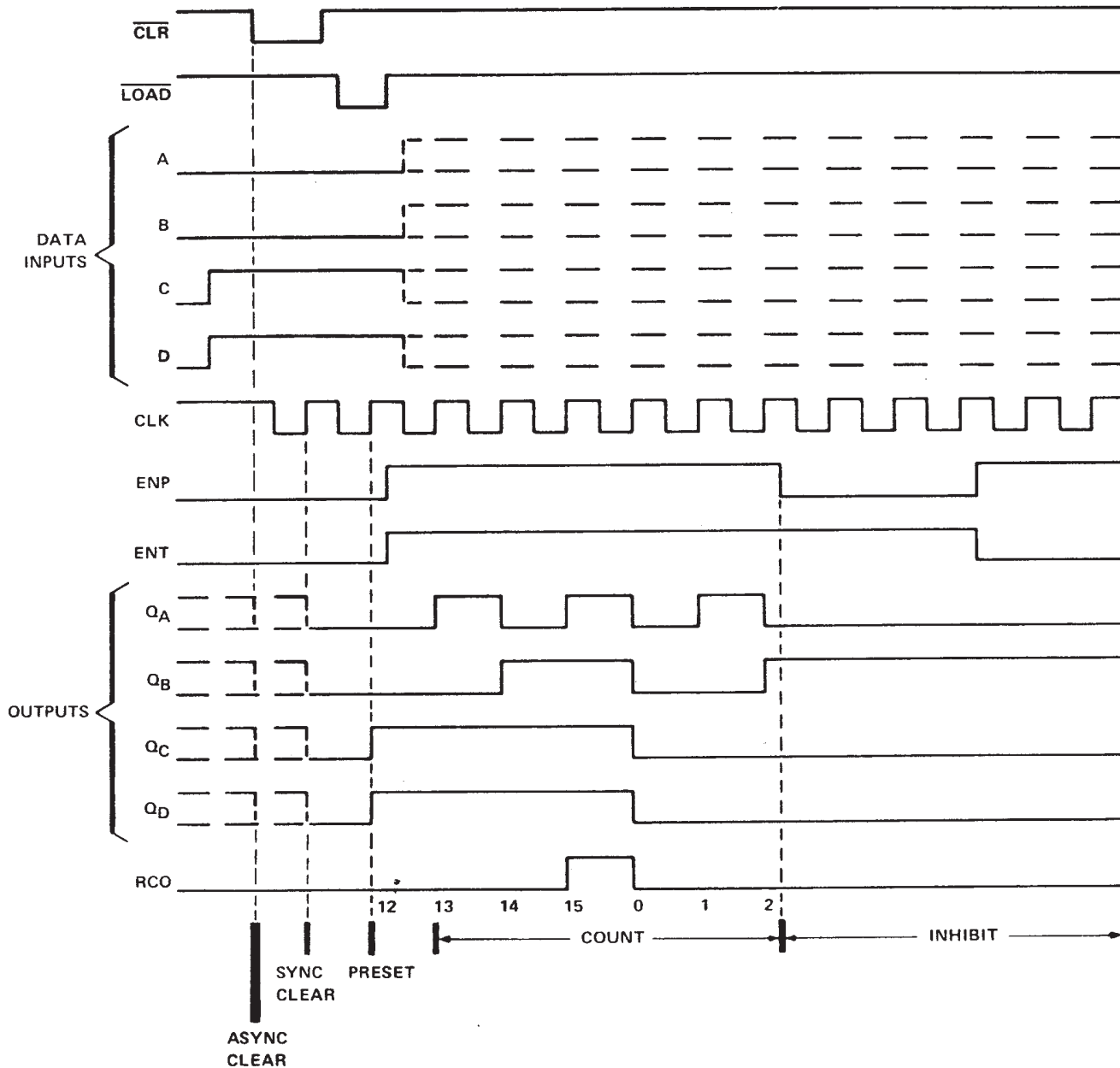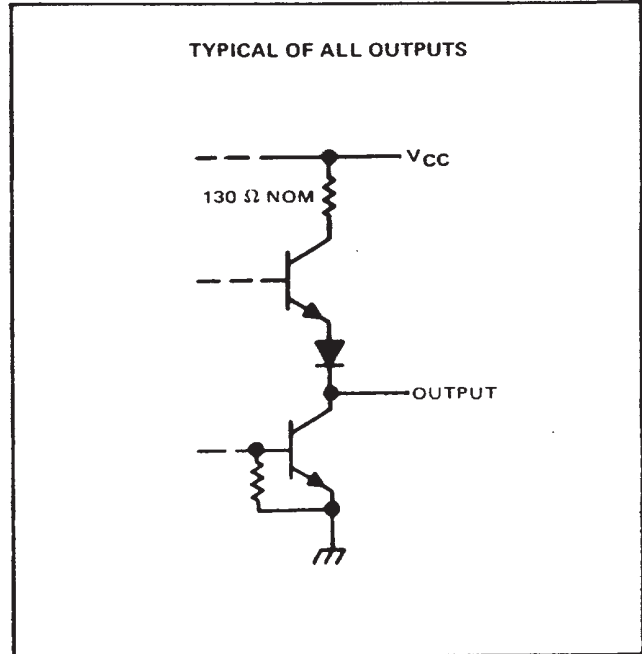Storage temperature range . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the count enable inputs P and T.

recommended operating conditions

		SN54160, SN54161 SN54162, SN54163			SN74160, SN74161 SN74162, SN74163			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$		25			25			ns
Width of clear pulse, $t_{w(clear)}$		20			20			ns
Setup time, t_{su} (see Figures 1 and 2)	Data inputs A, B, C, D	20			20			
	ENP	20			20			
	LOAD	25			25			ns
	$\overline{\text{CLR}}$ †	20			20			
Hold time at any input, t_h		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

†This applies only for '162 and '163, which have synchronous clear inputs.

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[†]	SN54160, SN54161 SN54162, SN54163			SN74160, SN74161 SN74162, SN74163			UNIT
			MIN	TYP[‡]	MAX	MIN	TYP[‡]	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 µA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current — CLK or ENT	V_{CC} = MAX, V_I = 2.4 V			80			80	µA
	High-level input current — Other inputs				40			40	
I_{IL}	Low-level input current — CLK or ENT	V_{CC} = MAX, V_I = 0.4 V			−3.2			−3.2	mA
	Low-level input current — Other inputs				−1.6			−1.6	
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−57	−18		−57	mA
I_{CCH}	Supply current, all outputs high	V_{CC} = MAX, See Note 3		59	85		59	94	mA
I_{CCL}	Supply current, all outputs low	V_{CC} = MAX, See Note 4		63	91		63	101	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTES: 3. I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.
      4. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}				25	32		MHz
t_{PLH}	CLK	RCO			23	35	ns
t_{PHL}	CLK	RCO			23	35	
t_{PLH}	CLK ($\overline{LOAD}$ input high)	Any Q	C_L = 15 pF, R_L = 400 Ω, See Figures 1 and 2 and Note 5		13	20	ns
t_{PHL}	CLK ($\overline{LOAD}$ input high)	Any Q			15	23	
t_{PLH}	CLK ($\overline{LOAD}$ input low)	Any Q			17	25	ns
t_{PHL}	CLK ($\overline{LOAD}$ input low)	Any Q			19	29	
t_{PLH}	ENT	RCO			11	16	ns
t_{PHL}	ENT	RCO			11	16	
t_{PHL}	$\overline{CLR}$	Any Q			26	38	ns

¶ f_{max} = Maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output
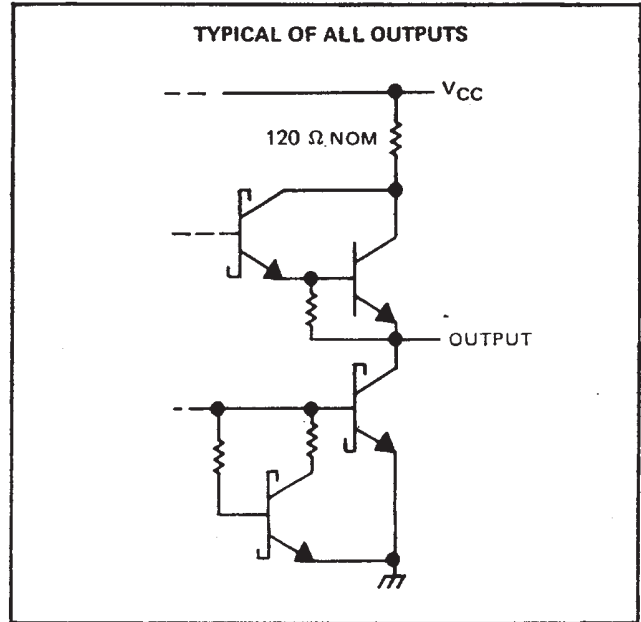t_{PHL} = propagation delay time, high-to-low-level output
NOTE 5: Propagation delay for clearing is measured from the clear input for the '160 and '161 or from the clock input transition for the '162 and '163.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

Data: R_{eq} = 25 kΩ NOM
CLK, ENT, $\overline{LOAD}$: R_{eq} = 10 kΩ NOM
ENP: R_{eq} = 20 kΩ NOM
$\overline{CLR}$ ('LS160A, 'LS161A): R_{eq} = 20 kΩ NOM
$\overline{CLR}$ ('LS162A, 'LS163A): R_{eq} = 10 kΩ NOM

TYPICAL OF ALL OUTPUTS

120 Ω NOM

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 7) . . . . 7 V
Input voltage . . . . 7 V
Operating free-air temperature range: SN54LS' Circuits . . . . −55°C to 125°C
                       SN74LS' Circuits . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C

NOTE 7: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54LS'			SN74LS'			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current				−400			−400	μA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		25	0		25	MHz
$t_{w(clock)}$	Width of clock pulse		25			25			ns
$t_{w(clear)}$	Width of clear pulse		20			20			ns
t_{su}	Setup time, (see Figures 1 and 2)	Data inputs A, B, C, D	20			20			ns
		ENP or ENT	20			20			
		$\overline{LOAD}$	20			20			
		$\overline{LOAD}$ inactive state	20			20			
		$\overline{CLR}$[†]	20			20			
		$\overline{CLR}$ inactive state	25			25			
t_h	Hold time at any input		3			3			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

† This applies only for 'LS162 and 'LS163, which have synchronous clear inputs.

TEXAS
INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS' MIN	SN54LS' TYP‡	SN54LS' MAX	SN74LS' MIN	SN74LS' TYP‡	SN74LS' MAX	UNIT
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	$I_I = -18$ mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, $V_{IL} = V_{IL}$ max, $I_{OH} = -400 \mu A$		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, $V_{IL} = V_{IL}$ max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	Data or ENP	V_{CC} = MAX, V_I = 7 V			0.1			0.1	mA
		$\overline{LOAD}$, CLK, or ENT				0.2			0.2	
		$\overline{CLR}$ ('LS160A, 'LS161A)				0.1			0.1	
		$\overline{CLR}$ ('LS162A, 'LS163A)				0.2			0.2	
I_{IH}	High-level input current	Data or ENP	V_{CC} = MAX, V_I = 2.7 V			20			20	μA
		$\overline{LOAD}$, CLK, or ENT				40			40	
		$\overline{CLR}$ ('LS160A, 'LS161A)				20			20	
		$\overline{CLR}$ ('LS162A, 'LS163A)				40			40	
I_{IL}	Low-level input current	Data or ENP	V_{CC} = MAX, V_I = 0.4 V			−0.4			−0.4	mA
		$\overline{LOAD}$, CLK, or ENT				−0.8			−0.8	
		$\overline{CLR}$ ('LS160A, 'LS161A)				−0.4			−0.4	
		$\overline{CLR}$ ('LS162A, 'LS163A)				−0.8			−0.8	
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CCH}	Supply current, all outputs high	V_{CC} = MAX, See Note 3			18	31		18	31	mA
I_{CCL}	Supply current, all outputs low	V_{CC} = MAX, See Note 4			19	32		19	32	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, $T_A = 25°C$.

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTES: 3. I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.

4. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

switching characteristics, V_{CC} = 5 V, $T_A = 25°C$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}				25	32		MHz
t_{PLH}	CLK	RCO			20	35	ns
t_{PHL}					18	35	
t_{PLH}	CLK ($\overline{LOAD}$ input high)	Any Q	C_L = 15 pF, R_L = 2 kΩ, See figures 1 and 2 and Note 8		13	24	ns
t_{PHL}					18	27	
t_{PLH}	CLK ($\overline{LOAD}$ input low)	Any Q			13	24	ns
t_{PHL}					18	27	
t_{PLH}	ENT	RCO			9	14	ns
t_{PHL}					9	14	
t_{PHL}	$\overline{CLR}$	Any Q			20	28	ns

¶f_{max} = Maximum clock frequency

t_{PLH} = propagation delay time, low-to-high-level output.

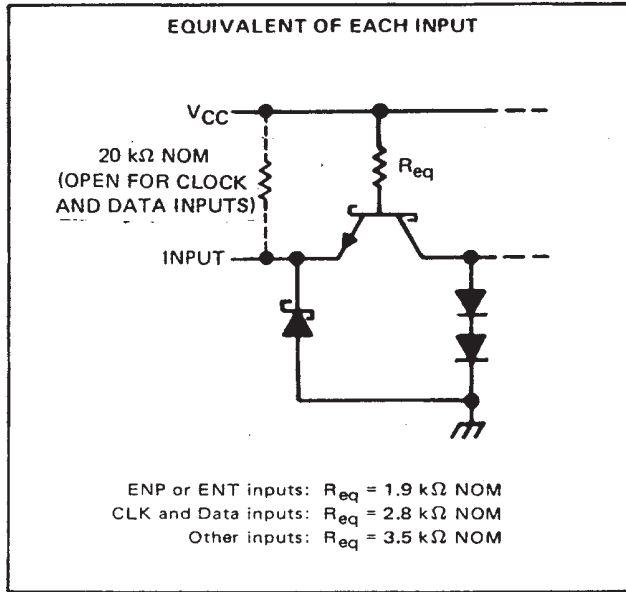t_{PHL} = propagation delay time, high-to-low-level output.

NOTE 8: Propagation delay for clearing is measured from the clear input for the 'LS160A and 'LS161A or from the clock transition for the 'LS162A and 'LS163A.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

V_{CC}

20 kΩ NOM
(OPEN FOR CLOCK
AND DATA INPUTS)

R_{eq}

INPUT

ENP or ENT inputs: R_{eq} = 1.9 kΩ NOM
CLK and Data inputs: R_{eq} = 2.8 kΩ NOM
Other inputs: R_{eq} = 3.5 kΩ NOM

TYPICAL OF ALL OUTPUTS

V_{CC}

50 Ω NOM

OUTPUT

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . 5.5 V
Operating free-air temperature range: SN54S162, SN54S163 (see Note 10) . . . . −55°C to 125°C
           SN74S162, SN74S163 . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C

recommended operating conditions

		SN54S162, SN54S163			SN74S162, SN74S163			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−1			1	mA
Low-level output current, I_{OL}				20			20	mA
Clock frequency, f_{clock}		0		40	0		40	MHz
Width of clock pulse, $t_{w(clock)}$ (high or low)		10			10			ns
Width of clear pulse, $t_{w(clear)}$		10			10			ns
Setup time, t_{su} (see Figure 4)	Data inputs, A, B, C, D	4			4			ns
	ENP or ENT	12			12			
	LOAD	14			14			
	CLR	14			14			
	LOAD inactive-state	12			12			
	CLR inactive-state	12			12			
Release time, $t_{release}$ (see Figure 4)	ENP or ENT			4			4	ns
Hold time, t_h (see Figure 4)	Data inputs A, B, C, D	3			3			ns
	LOAD	0			0			
	CLR	0			0			
Operating free-air temperature, T_A (see Note 10)		55		125	0		70	C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
       2. This is the voltage between two emitters of a multiple emitter transistor. For these circuits, this rating applies between the count enable inputs P and T.
    10. An SN54S162 or SN54S163 in the W package operating at free air temperatures above 91 C requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 26°C/W.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[†]	SN54S162 SN54S163			SN74S162 SN74S163			UNIT
			MIN	TYP[‡]	MAX	MIN	TYP[‡]	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.5			0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	CLK and data inputs	V_{CC} = MAX, V_I = 2.7 V			50			50	µA
		Other inputs		−10		−200	−10		−200	
I_{IL}	Low-level input current	ENT	V_{CC} = MAX, V_I = 0.5 V			−4			−4	mA
		Other inputs				2			2	
I_{OS}	Short-circuit output current[§]	V_{CC} = MAX	−40		−100	−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX		95	160		95	160	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
[‡] All typical values are at V_{CC} 5 V, T_A 25 C.
[§] Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER[¶]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L 15 pF, R_L = 280 Ω, See Figures 1, 3, and 4	40	70		MHz
t_{PLH}	CLK	RCO			14	25	ns
t_{PHL}					17	25	
t_{PLH}	CLK	Any Q			8	15	ns
t_{PHL}					10	15	
t_{PLH}	ENT	RCO			10	15	ns
t_{PHL}					10	15	

[¶] f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low to high level output
t_{PHL} ≡ propagation delay time, high to low level output

TEXAS
INSTRUMENTS

SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A, SN54S162,
SN54S163, SN74160 THRU SN74163, SN74LS160A THRU SN74LS163A,
SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

SDLS060 – OCTOBER 1976 – REVISED MARCH 1988

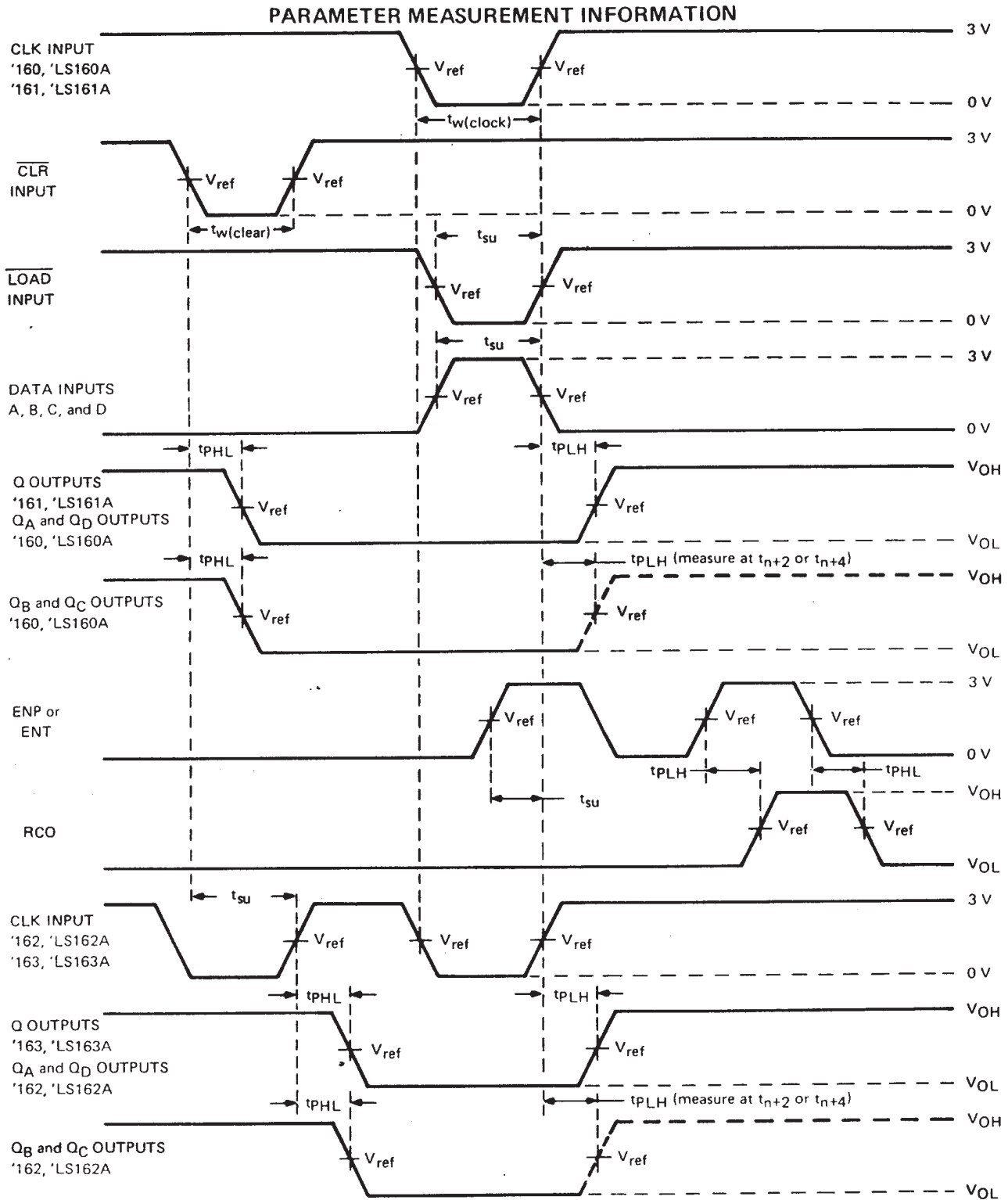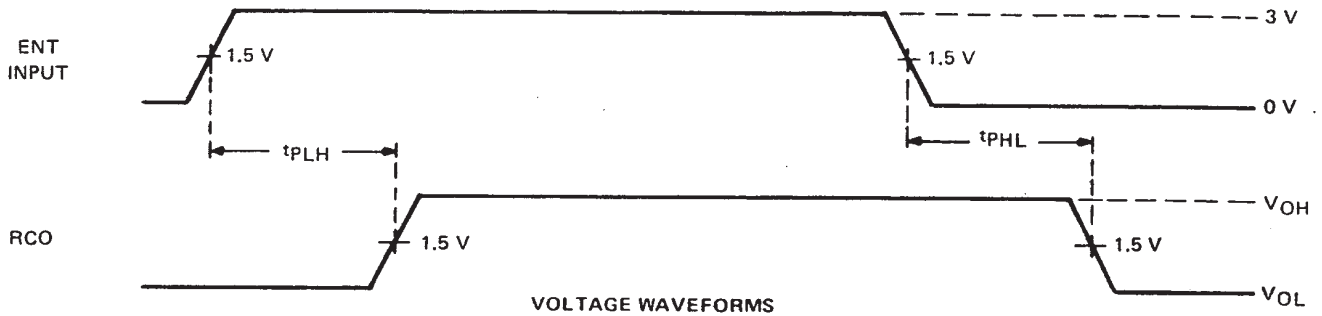## PARAMETER MEASUREMENT INFORMATION
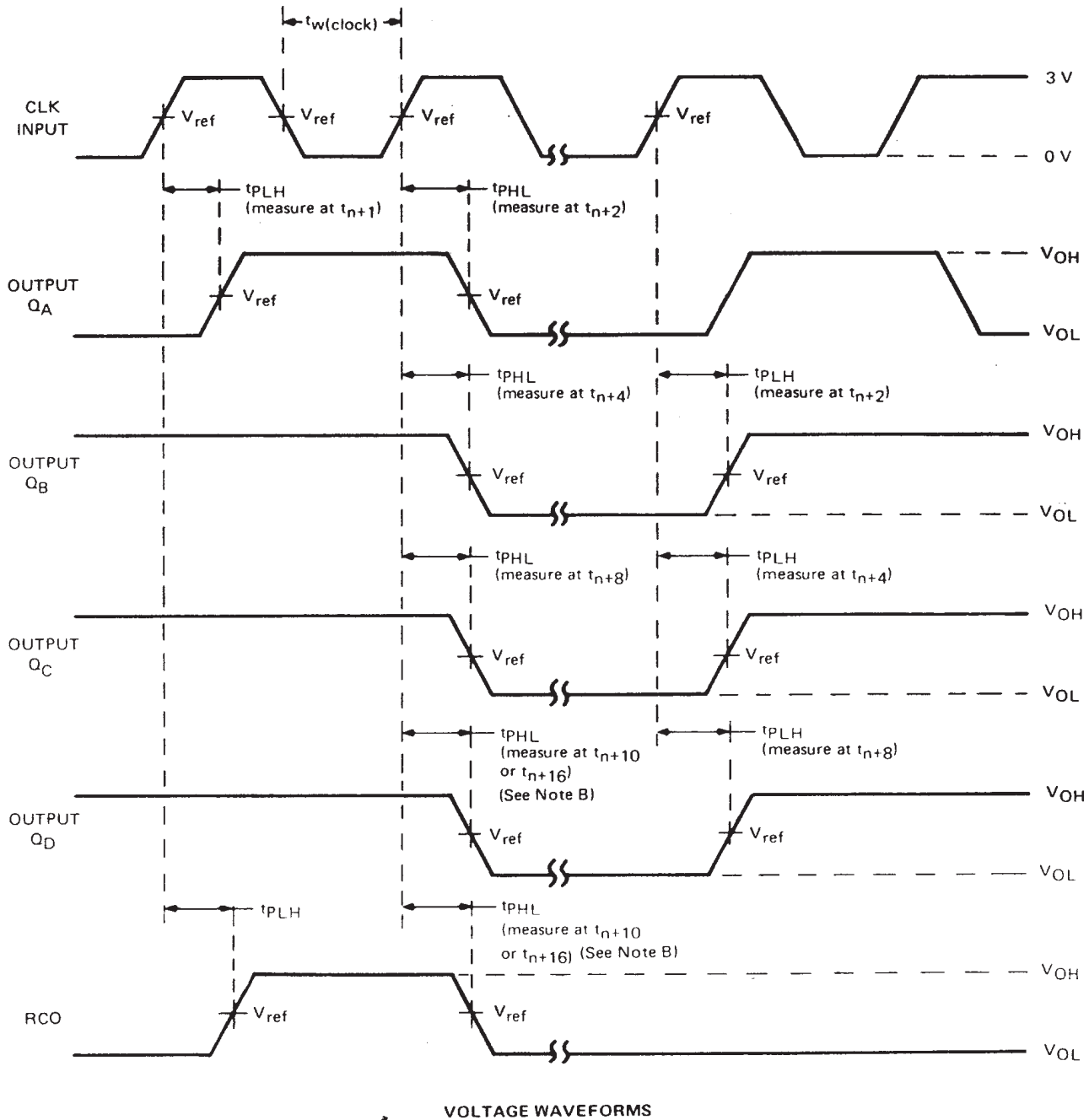
VOLTAGE WAVEFORMS

NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50 \, \Omega$; for '160 thru '163, $t_r \le 10$ ns, $t_f \le 10$ ns; for 'LS160A thru 'LS163A $t_r \le 15$ ns, $t_f \le 6$ ns; and for 'S162, 'S163, $t_r \le 2.5$ ns, $t_f \le 2.5$ ns. Vary PRR to measure f_{max}.

B. Outputs Q_D and carry are tested at t_{n+10} for '160, '162, 'LS160A, 'LS162A, and 'S162, and at t_{n+16} for '161, '163, 'LS161A, 'LS163A, and 'S163, where t_n is the bit time when all outputs are low.

C. For '160 thru '163, 'S162, and 'S163, $V_{ref} = 1.5$ V; for 'LS160A thru 'LS163A, $V_{ref} = 1.3$ V.

FIGURE 1—SWITCHING TIMES

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A,
SN74160 THRU SN74163, SN74LS160A THRU SN74LS163A,
SYNCHRONOUS 4-BIT COUNTERS

SDLS060 – OCTOBER 1976 – REVISED MARCH 1988

PARAMETER MEASUREMENT INFORMATION

VOLTAGE WAVEFORMS

NOTES: A. The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$;
for '160 thru '163, $t_r \le 10$ ns, $t_f \le 10$ ns; and for 'LS160A thru 'LS163A, $t_r \le 15$ ns, $t_f \le 6$ ns.

B. Enable P and enable T setup times are measured at t_{n+0}.

C. For '160 thru '163, $V_{ref} = 1.5$ V; for 'LS160A thru 'LS163A, $V_{ref} = 1.3$ V.

FIGURE 2–SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION

VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \approx 2.5$ ns, $t_f \approx 2.5$ ns, PRR ≈ 1 MHz, duty cycle $\approx 50\%$, $Z_{out} \approx 50 \, \Omega$.

B. t_{PLH} and t_{PHL} from enable T input to carry output assume that the counter is at the maximum count (Q_A and Q_D high for 'S162, all Q outputs high for 'S163).

FIGURE 3–PROPAGATION DELAY TIMES FROM ENABLE T INPUT TO CARRY OUTPUT

VOLTAGE WAVEFORMS
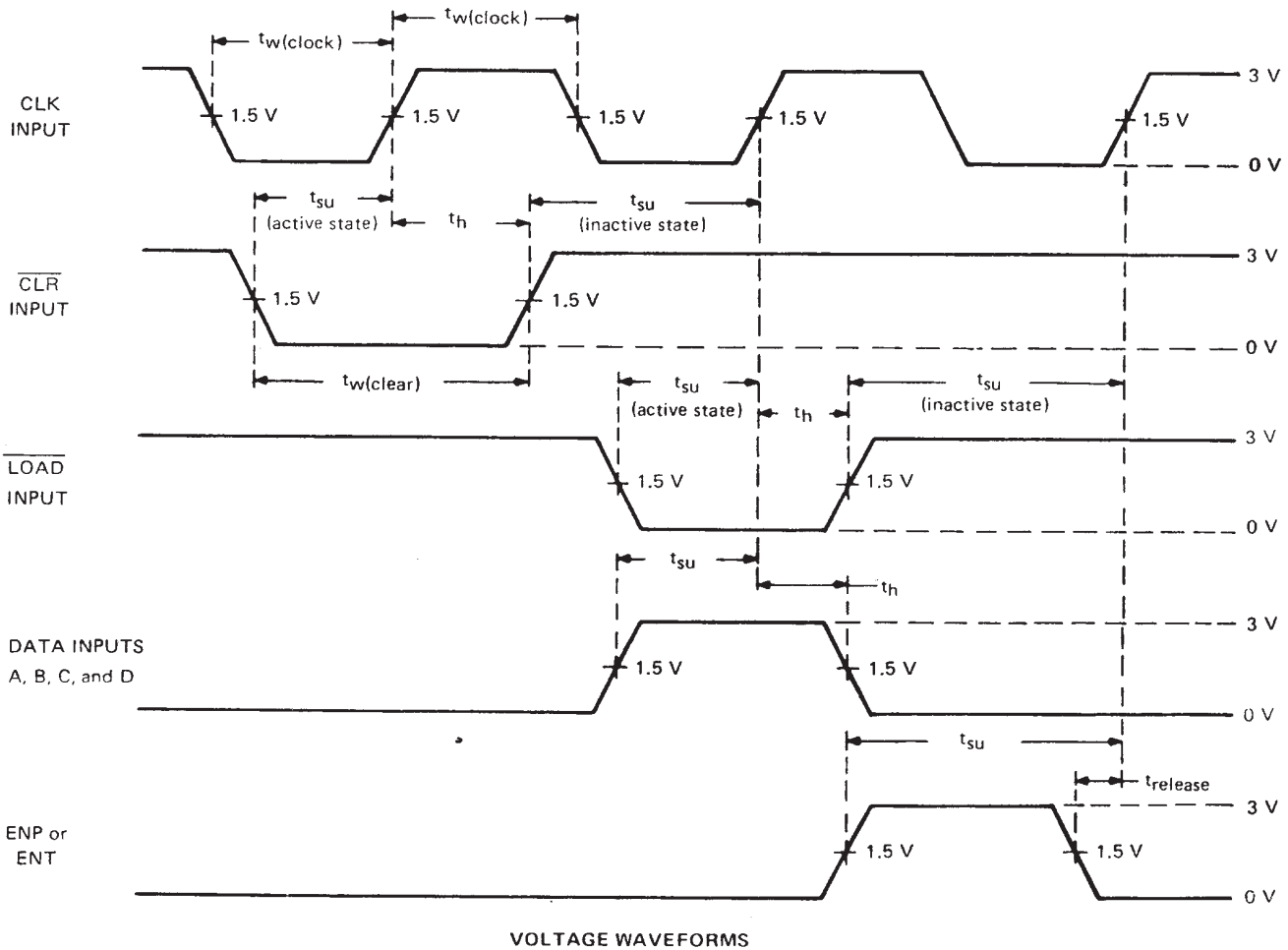
NOTE A: The input pulses are supplied by generators having the following characteristics: $t_r \approx 2.5$ ns, $t_f \approx 2.5$ ns, PRR ≈ 1 MHz, duty cycle $\approx 50\%$, $Z_{out} \approx 50 \, \Omega$.

FIGURE 4–PULSE WIDTHS, SETUP TIMES, HOLD TIMES, AND RELEASE TIME

TEXAS INSTRUMENTS
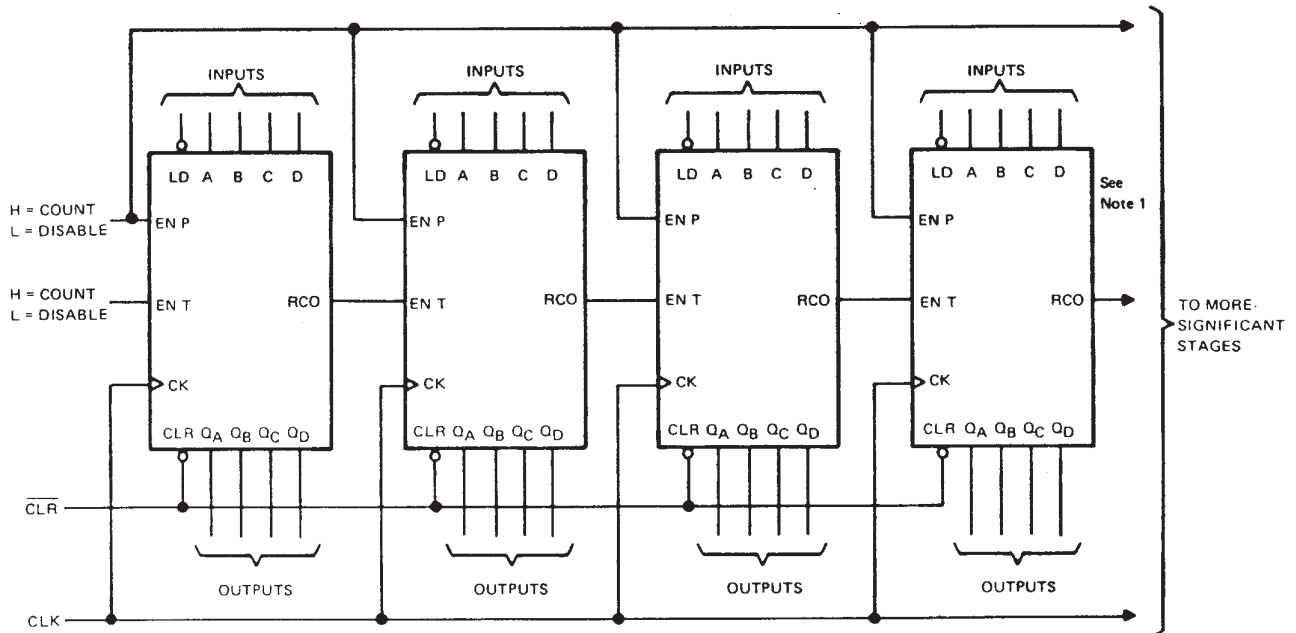
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A, SN54S162,
SN54S163, SN74160 THRU SN74163, SN74LS160A THRU SN74LS163A,
SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

SDLS060 – OCTOBER 1976 – REVISED MARCH 1988

TYPICAL APPLICATION DATA

This application demonstrates how the ripple mode carry circuit (Figure 1) and the carry-look-ahead circuit (Figure 2) can be used to implement a high-speed N-bit counter. The '160, '162, 'LS160A, 'LS162A, or 'S162 will count in BCD and the '161, '163, 'LS161A, 'LS163A, or 'S163 will count in binary. When additional stages are added the f_{MAX} decreases in Figure 1, but remains unchanged in Figure 2.

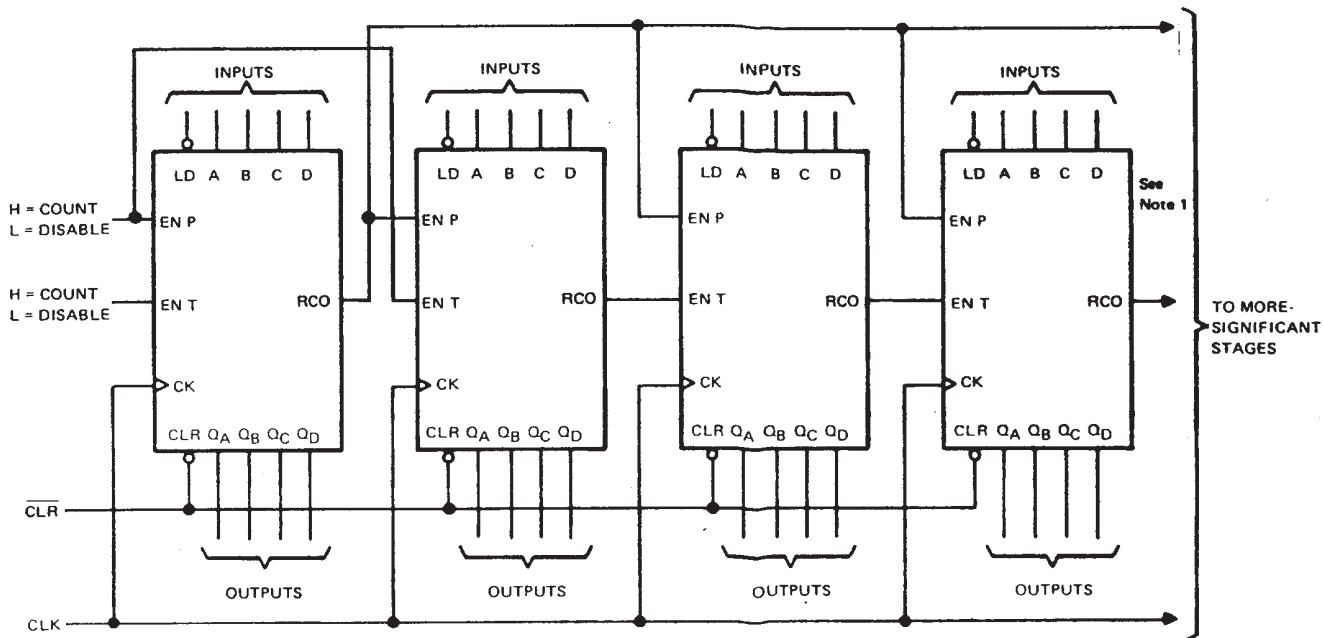### N-BIT SYNCHRONOUS COUNTERS

$$f_{MAX} = 1/(\text{CLK to RCO } t_{PLH}) + (\text{ENT to RCO } t_{PLH})(N-2) + (\text{ENT } t_{su})$$

FIGURE 1

SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A, SN54S162, SN54S163, SN74160 THRU SN74163, SN74LS160A THRU SN74LS163A, SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

SDLS060 – OCTOBER 1976 – REVISED MARCH 1988

TYPICAL APPLICATION DATA

$$f_{MAX} = 1/(\text{CLK to RCO } t_{PLH}) + (\text{ENP } t_{su})$$

FIGURE 2

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.