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NTE74110
Integrated Circuit
TTL – AND–Gated J–K Master–Slave Flip–Flop with Data Lockout

Description:

The NTE74110 is a DC coupled, variable–skew, J–K flip–flop in a 14–Lead plastic DIP type package that utilizes TTL circuitry to obtain 25MHz performance typically. It is termed “variable–skew” because it allows the maximum clock skew in a system to be a direct function of the clock pulse width. The J and K inputs are enabled only during a short period (20ns maximum setup time plus 5ns maximum hold time) on the rising edge of the clock pulse. After this, inputs may be changed while the clock is at the high level without affecting the state of the master. On the threshold level of the falling edge of the clock pulse, the data stored in the master during the rising edge will be transferred to the output. The effective allowable clock skew then is minimum propagation delay time minus hold time, plus clock pulse width. This means that the system designer can set the maximum allowable clock skew needed by varying the clock pulse width. Thus, system design is made easier and the requirements for sophisticated clock distribution systems are minimized or, in some cases, entirely eliminated. This flip–flop has an additional feature — the synchronous input has reduced sensitivity to data change while the clock is high because the data needs to be present for only a short period of time and the system’s susceptibility to noise is thereby effectively reduced.

The NTE74110 has the same functional advantages as the NTE7472 in that three–input AND logic is provided for both the J and K data functions. Preset and clear inputs, which are completely independent of the state of the clock, are also provided.

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7V
DC Input Voltage, V_{IN} 5.5V
Operating Temperature Range, T_A . . . . . 0°C to +70°C
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C

Note 1. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High−Level Input Voltage	V_{IH}	2.0	–	–	V
Low−Level Input Voltage	V_{IL}	–	–	0.8	V
High−Level Output Current	I_{OH}	–	–	−0.8	mA
Low−Level Output Current	I_{OL}	–	–	16	mA
Pulse Duration CLK High or Low	t_w	25	–	–	ns
$\overline{PRE}$ or $\overline{CLR}$ Low		25	–	–	ns
Input Setup Time before CLK↑	t_{su}	20	–	–	ns
Input Hold Time Data after CLK↑	t_h	5	–	–	ns
Operating Temperature Range	T_A	0	–	+70	°C

Electrical Characteristics: (Note 2, Note 3)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = −12mA	–	–	−1.5	V
High Level Output Voltage	V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −0.8mA	2.4	3.4	–	V
Low Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 16mA	–	0.2	0.4	V
Input Current	I_I	V_{CC} = MAX, V_I = 5.5V	–	–	1	mA
High Level Input Current J or K or CLK	I_{IH}	V_{CC} = MAX, V_I = 2.4V	–	–	40	μA
$\overline{CLR}$ or $\overline{PRE}$			–	–	160	μA
$\overline{PRE}$			–	–	160	μA
Low Level Input Current J or K or CLK	I_{IL}	V_{CC} = MAX, V_I = 0.4V	–	–	−1.6	mA
$\overline{CLR}$ (Note 4)			–	–	−3.2	mA
$\overline{PRE}$ (Note 4)			–	–	−3.2	mA
Short−Circuit Output Current	I_{OS}	V_{CC} = MAX, Note 5	−18	–	−57	mA
Supply Current	I_{CC}	V_{CC} = MAX, Note 6	–	20	34	mA

Note 2. .For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 3. All typical values are at V_{CC} = 5V, T_A = +25°C.

Note 4. Clear is tested with preset high and preset is tested with clear high.

Note 5. Not more than one output should be shorted at a time.

Note 6. With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is 4.5V.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Clock Frequency	t_{max}	R_L = 400Ω, C_L = 15pF	20	25	–	MHz
Propagation Delay Time (From $\overline{PRE}$ or $\overline{CLR}$ Input to Q or $\overline{Q}$ Output)	t_{PLH}		–	12	20	ns
	t_{PHL}		–	18	25	ns
Propagation Delay Time (From CLK Input to Q or $\overline{Q}$ Output)	t_{PLH}		–	20	30	ns
	t_{PHL}		–	13	20	ns

Function Table:

Inputs					Outputs	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	⎍	L	L	Q_0	$\overline{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	Toggle	

† This configuration is nonstable; that is, it will not persist when preset or clear return to their inactive (high) level.

Pin Connection Diagram