Timekeeping, DTMF Circuits

Watches

Part Number	Circuit Description	Typical Current at 1.55 VDC
ICM7245B/D/E/F ICM7245U	Analog quartz watch/clock circuit. ICM7245B/D/E/F for bipolar stepper motors. ICM7245U for unipolar stepper motors. Ultra high accuracy: 0.1 ppm.	0.4μA

Notes: All Intersil watch circuits are designed for use with a 32.768Hz quartz crystal. All provide a rapid advance setting
Watch circuits are normally sold in die form. The ICM7245B/D/E/F and ICM7245U are available in either an 8 pin plastic DIP or mini-flatpack as well as dice.
All Intersil watch circuits have a fixed on-chip oscillator capacitor. The above circuits show typical current at 1.55 Volts LCD units in doubler mode.

Dual Tone (Touch Tone) Encoders

Part Number	Circuit Description	Package	Crystal Frequency	Output
ICM7206	Touch-tone encoder; requires single contact per key.	16-Pin DIP	3.57954 MHz	2-of-8 sine wave for tone dialing
ICM7206A	Touch-tone encoder; requires one contact per key with common line connected to + supply.	16-Pin DIP	3.57954 MHz	2-of-8 sine wave for tone dialing
ICM7206B	Touch-tone encoder; requires 2 contacts per key with common line connected to negative supply; oscillator enabled when key is pressed.	16-Pin DIP	3.57954 MHz	2-of-8 sine wave for tone dialing
ICM7206C	Touch-tone encoder requires single contact per key; oscillator enabled only when key is depressed. Disable line tied to V^-	16-Pin DIP	3.57954 MHz	2-of-8 sine wave for tone dialing
ICM7206D	Touch tone encoder; requires single contact per key; oscillator enabled only when key is depressed. DISABLE line tied to $V+$.	16-Pin DIP	3.57954 MHz	2-of-8 sine wave for tone dialing

Clock and Timing Signal Generators

ICM7209	High-frequency clock-generator for 5-volt systems	8-Pin DIP	to 10 MHz	Crystal frequency, plus 8 divider stage
ICM7213	Oscillator and frequency divider	14-Pin DIP (plastic)	to 10 MHz	1pps, 1ppm, 10 Hz, composite

Clocks

Part Number	Circuit Description	Typical Operating Voltage	Package
ICM1115	Analog quartz clock circuit with simple alarm. For bipolar stepper motors; 1 Hz square wave output. $f_{osc} = 4.19MHz$	1.5V	8 pin DIP
ICM1115A	Analog quartz clock circuit with simple alarm. For bipolar stepper motors; 1 Hz square wave output. $f_{osc} = 4.19MHz$		
ICM1115B	Analog quartz clock circuit with simple alarm. For bipolar stepper motors; 1 Hz square wave output. $f_{osc} = 4.19MHz$		
ICM7038A	Analog quartz clock circuit with simple alarm. For synchronous motors.	3.0V	8 pin DIP
ICM7038B	Analog quartz clock circuit with simple alarm. For synchronous motors.	1.5V	8 pin DIP
ICM7050	Analog quartz clock circuit with complex alarm. For bipolar stepper motors. 47 ms pulse width. 1Hz rate. $f_{osc} = 4.19MHz$	1.5V	8 pin DIP
ICM7051A	Analog quartz clock circuit for automotive applications—synchronous motors. 64 Hz square wave.	12.0V	8 pin DIP
ICM7051B	Analog quartz clock circuit for automotive applications—bipolar stepper motors. 31 ms pulse width. 1Hz rate		
ICM7070L	Analog quartz clock circuit with complex alarm. For bipolar stepper motors, 31 ms pulse width @ 0.5 Hz. $f_{osc} = 32$ kHz	1.5	8 pin DIP
ICM7223	4 Digit LCD Alarm Clock with Snooze.	1.5V	40 pin DIP
ICM7223D	Direct drive Cricket alarm. 24 hour format by bond option. For 32.768 kHz quartz crystal.		
ICM7223A	4 Digit LCD Clock Radio circuit with Sleep Timer. Snooze and Alarm. Low battery indicator. Radio Enable. For 32.768 kHz quartz crystal.	9.0V	40 pin DIP
ICM7223VF	4 Digit Vacuum Fluorescent Clock Radio/Auto Clock circuit with Sleep Timer. Alarm. Snooze. and Radio Enable. For 32.768 kHz quartz crystal.	12.0V	40 pin DIP

Notes: All Analog clock circuits are designed for use with a 4.19 MHz quartz crystal, with the exception of the ICM7223 series which uses a 32.768 kHz crystal.
Clock circuits are normally purchased in package form; each is also available as dice.
All Analog clock circuits are mask programmable for oscillator frequency, output frequency and pulse width, and alarm frequency. Consult the factory for details.

Stopwatches

Part Number	Circuit Description	Crystal Frequency	Package
ICM7045	8 Digit 4 Function LED stopwatch circuit. Features Hours:Minutes:Seconds:100ths. Provides Time Out. Taylor. Split and Rally modes. Direct drive for LEDs. May be used as 24-hour clock.	6.55 MHz	28 pin DIP
ICM7215	6 Digit 4 Function LED stopwatch circuit. Features Minutes:Seconds:100ths. Provides Time out. Taylor and Split modes. Direct drive for LEDs.	3.28 MHz	24 pin DIP

Notes: All stopwatches may be purchased as an Evaluation Kit (EV KIT) which includes the IC and the appropriate quartz crystal. All operate at 2.5 to 4.5 volts, and source 15 mA current to the segments of the LEDs.

INTERSIL

CMOS OSCILLATOR/DIVIDER/DRIVERS
SELECTION GUIDE

(Includes circuits used in quartz analog clock and watch applications)

PRODUCT NUMBER	MASK VARIANT	CRYSTAL FREQUENCY (MHz)	MOTOR DRIVE OUTPUT	OUTPUT PULSE CHARACTERISTICS Width (ms)	Freq. (pulses per sec)	ALARM FREQUENCY (Hz)	NOMINAL VOLTAGE (V)	TYPICAL CURRENT (μA)	PACKAGE[4]
ICM7038A	—	4.19	Synchronous	7.8 [1]	64	512	3.0	90	8-pin DIP
ICM7038B	—	4.19	Synchronous	7.8 [1]	64	512	1.5	40	8-pin DIP
ICM7213	—	4.19	Multiple	7.8 31.2 125.	1 16 1 per min.	1024+16+2	3.0	100	14-pin DIP
ICM7050A	ITS9044-1	4.19	Unipolar	15.6	1	1024	1.5	40	8-pin DIP
ICM7050	—	4.19	Bipolar	46.9	0.5	2048+8+1	1.5	40	8-pin DIP
ICM7051A	ITS9042-1	4.19	Bipolar	7.8[1]	64	—	4.5-13.5	500	8-pin DIP
ICM7051B	—	4.19	Bipolar	31.2	0.5	—	4.5-13.5	500	8-pin DIP
ICM7070L[2]	—	32 kHz	Bipolar	31.2	0.5	2048+8+1	1.5	3	8-pin DIP
ICM7245A[2]	—	32 kHz	Bipolar	9.7	0.5	—	1.5	0.4	8-pin DIP
ICM7245B[2]	—	32 kHz	Bipolar	7.8	0.5	—	1.5	0.4	8-pin DIP
ICM7245D[2]	—	32 kHz	Bipolar	7.8	1 per 10 sec	—	1.5	0.4	8-pin DIP
ICM7245E[2]	—	32 kHz	Bipolar	7.8	1 per 12 sec	—	1.5	0.4	8-pin DIP
ICM7245F[2]	—	32 kHz	Bipolar	7.8	1 per 20 sec	—	1.5	0.4	8-pin DIP
ICM7245U[2]	—	32 kHz	Unipolar	3.9	1	—	1.5	0.4	8-pin DIP
ICM1115A	—	4.19	Bipolar	1000[1]	0.5	64	1.5	80	8-pin DIP
ICM1115B	—	4.19	Bipolar	1000[1]	0.5	64	1.5	40	8-pin DIP

7

All Intersil analog quartz products are mask programmable. Options include:

- Crystal frequency (32 kHz, 1 MHz, etc.)
- Pulse width (500 msec to 3.9 msec)
- Pulse frequency (64 Hz to 0.5 Hz)
- Alarm frequency (64 Hz to 4096 Hz, including complex)
- Motor drive characteristics
- Oscillator characteristics, including fixed capacitors (ICM7050

Notes: [1] Square Wave.
[2] Includes a fixed value capacitor on oscillator input.
[3] Includes snooze.
[4] All Intersil analog quartz products may be ordered in die form.

ICM7038 Family CMOS Analog Quartz Clock Circuit

Synchronous Motor Applications

FEATURES

- **Battery operation: 1.2 to 3.6V devices**
- **Very low power: 30μA typical (1.5V parts)**
- **High output current drive: 1 mA minimum**
- **Zero output bridge DC component (50% duty cycle square wave)**
- **All inputs fully protected — no special handling precautions required**
- **Wide operating temperature range: −20°C to +70°C**

GENERAL DESCRIPTION

The ICM7038 family of synchronous motor drivers is designed to operate from a 1.5V battery, and performs the functions of oscillator, frequency divider and output driver. In addition a power driver is tapped off from the thirteenth divider for use as an alarm driver.

Specifically the ICM7038 family uses an inverter oscillator having all biasing components on chip. Binary dividers permit frequency division from 4 MHz down to 64 Hz. The output from the divider network drives a bridge output circuit which provides a 50% duty cycle AC square wave having virtually zero DC component for driving a synchronous single phase motor. The total output drivers saturation is typically 200 ohms providing efficient operation of synchronous motors. The alarm output will drive a transducer (piezoelectric or speaker).

TABLE OF OPTIONS

The ICM7038 may be modified with alternative metal masks to provide any number of binary divider stages up to a maximum of 19 and supply voltages from 1.2 V to over 3.6V together with various output options. Consult your Intersil representative or the factory for further information. The alarm output can be tapped off from any of the latter divider stages.

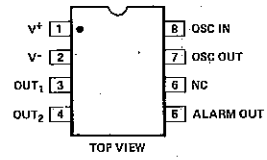
(See table for standard options).

Part Number	Binary Dividers	Nominal Output Frequency	Nominal Supply Voltage
ICM7038A	16	64 Hz	3.0V
ICM7038B	16	64 Hz	1.5V

7

PIN CONFIGURATION

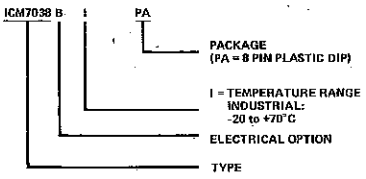
(OUTLINE DRAWING PA)



TOP VIEW

PIN 1 IS DESIGNATED BY EITHER A DOT OR A NOTCH.

ORDERING INFORMATION



ORDER DEVICES BY FOLLOWING PART NUMBER—
ICM7038B I PA

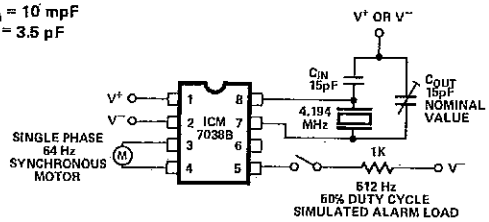
ABSOLUTE MAXIMUM RATINGS

Power Dissipation Output Short Circuit(1) 300mW
Supply Voltage:
ICM7038A 5V
ICM7038B 3V
Output Voltage(2) ..... V^- to V^+
Input Voltage(2) ..... V^- to V^+
Storage Temperature ..... −30°C to +125°C
Operating Temperature ..... −20°C to +70°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

TEST CIRCUIT

QUARTZ CRYSTAL PARAMETERS
f = 4,194,304 Hz
R_S = 35Ω
C_m = 10 mpF
C_0 = 3.5 pF



NOTES:
1. This value of power dissipation refers to that of the package and will not be obtained under normal operating conditions.
2. Except for instantaneous static discharges all terminals may exceed the supply voltage (2.0V max) by ±0.5 volt provided that the currents in these terminals are limited to 2 mA each.

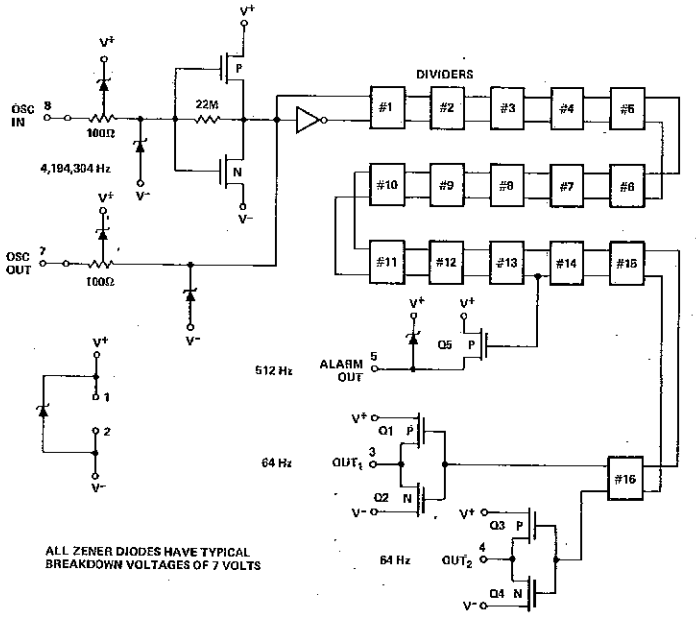
OPERATING CHARACTERISTICS

(V^+ = 3.0V (ICM7038A) or 1.5V (ICM7038B), f_{osc} = 4,194,304 Hz, test circuit 1, T_A = 25°C, unless otherwise specifed.

Parameter	Symbol	Conditions	7038A/C/F			7038B/D/E/G			
			Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
Supply Current	I^+			90	150		30	60	μA
Guaranteed Operating Voltage Range	V^+	−20°C ≤ to ≤ 70°C	2.2		3.6	1.2		1.8	V
Total Output Saturation Resistance	R_{SAT}	p + n Output Transistors, I_{OUT} = 0.5mA		230	400		200	700	Ω
Alarm Output Saturation Resistance	R_{AL}	I_{OUT} = 1mA		200	400		300	800	Ω
Oscillator Stability	f_{STAB}	Over V^+ range $C_{IN} = C_{OUT}$ = 15pF		1			1		ppm
Oscillator Start-Up Time	t_{START}	V^+ = min.			1.0			1.0	sec

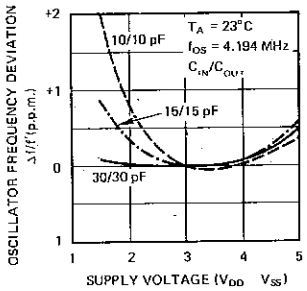
7

SCHEMATIC DIAGRAM (ICM7038B)

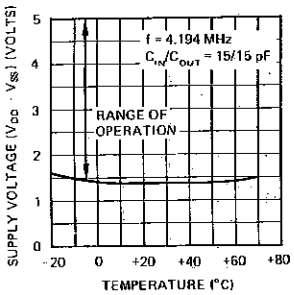


TYPICAL OPERATING CHARACTERISTICS (ICM7038A)

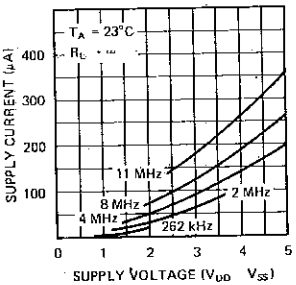
OSCILLATOR STABILITY VS. SUPPLY VOLTAGE



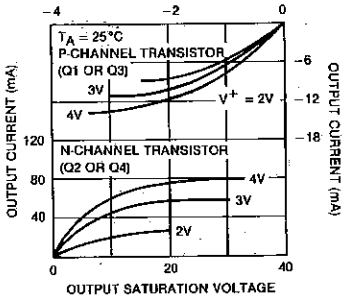
MINIMUM OPERATING SUPPLY VOLTAGE VS. TEMPERATURE



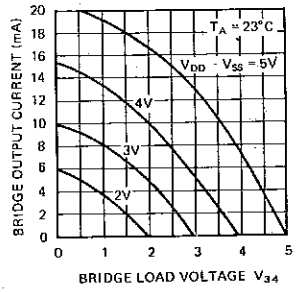
SUPPLY CURRENT VS. SUPPLY VOLTAGE



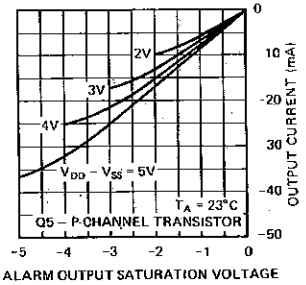
OUTPUT CURRENT VS. OUTPUT SATURATION VOLTAGE



BRIDGE OUTPUT CURRENT VS. BRIDGE OUTPUT VOLTAGE

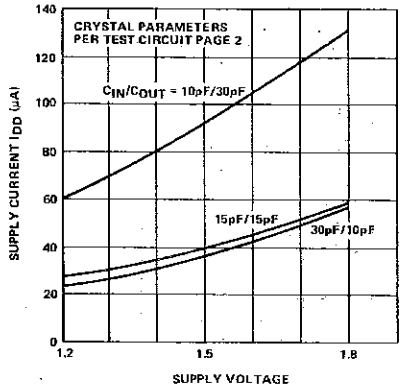


ALARM OUTPUT CURRENT (SOURCE) VS. OUTPUT SATURATION VOLTAGE

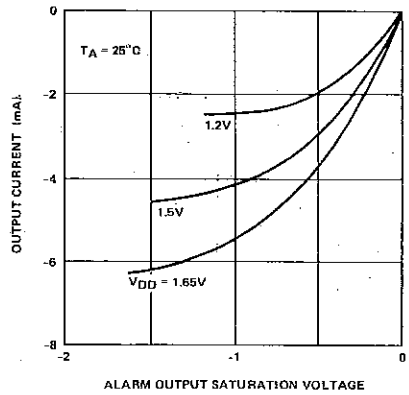


TYPICAL OPERATING CHARACTERISTICS (ICM7038B)

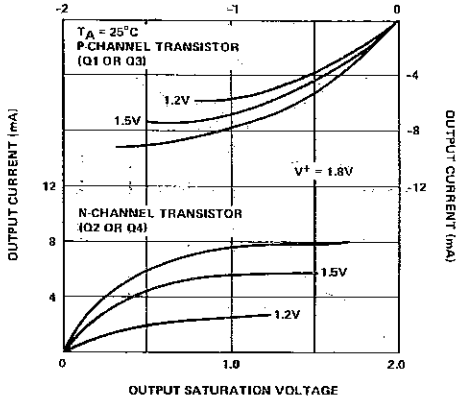
SUPPLY CURRENT VS. SUPPLY VOLTAGE



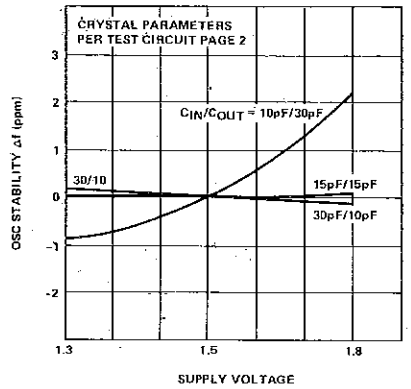
ALARM OUTPUT CURRENT (SOURCE) VS. OUTPUT SATURATION VOLTAGE



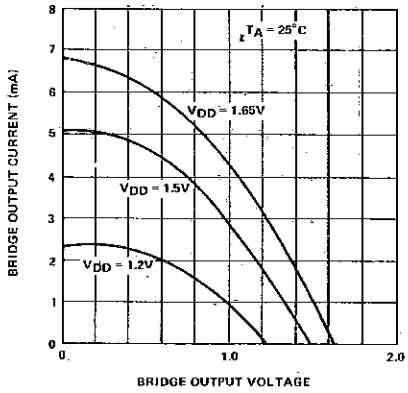
OUTPUT CURRENT (SOURCE) VS. OUTPUT SATURATION VOLTAGE



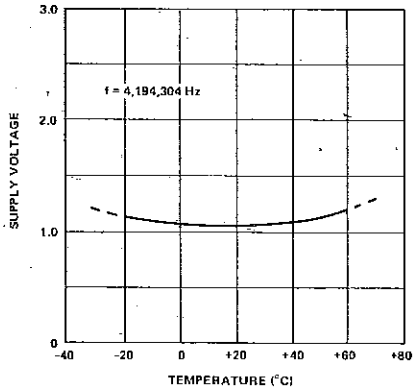
OSCILLATOR STABILITY VS. SUPPLY VOLTAGE



BRIDGE OUTPUT CURRENT VS. BRIDGE OUTPUT VOLTAGE



MINIMUM OPERATING SUPPLY VOLTAGE VS. TEMPERATURE

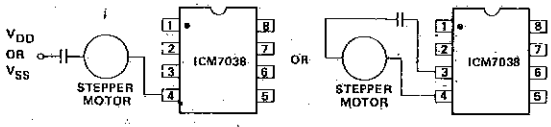


7

APPLICATION NOTES

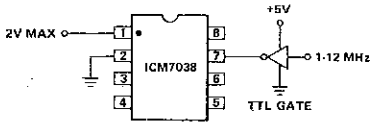
GENERAL DESCRIPTION

The ICM7038 Family has been designed primarily for quartz clock and timer applications using oscillator frequencies between 2.0 and 10 MHz. The design objectives were exceptional oscillator frequency stability, very low power, wide supply voltage range and wide temperature range. The oscillator contains all components except the tuning components and quartz crystal. Three outputs are provided. The two principal outputs are intended to be used to drive a single phase synchronous motor in a bridge configuration. As such, because of the matching of the transistors in the two outputs, the output DC component is extremely small. Stepper motors may also be used by placing a capacitor in series with the motor and using either a single output or the bridge output.



Alternatively outputs 3 and 4 may be used to drive TTL logic directly for timer applications.

The alarm output is taken from the output of the thirteenth divider and can source 1 mA at a low saturation voltage.



The ICM7038 may be used as a straight divider by driving directly into the oscillator output (pin no. 7) with a low impedance square wave drive. As such it may be used over the frequency range 1 MHz to 10 MHz.

OSCILLATOR CONSIDERATIONS

The oscillator of the ICM7038 is designed to operate with crystals having a load capacitance of 10 to 12 pF. This allows nominal capacitor values of 15/15 pF or 20/20 pF. Increasing the load capacitance of the crystal requires larger oscillator device sizes, which causes the supply current to increase. Modifications to the oscillator can be made on a custom basis. The tuning range can be increased by using crystals with lower load capacitances, however, the stability may decrease somewhat. This can be counteracted by reducing the motional capacitance of the crystal. A non-linear feedback resistor is provided on chip, which has a maximum value at start up. Oscillator tuning should be done at the oscillator output.

The following expressions can be used to arrive at a crystal specification:

Tuning Range

$$\frac{\Delta f}{f} = \frac{C_m}{2(C_O + C_L)} \qquad C_L = \frac{C_{IN}C_{OUT}}{C_{IN}+C_{OUT}}$$

g_m required for startup

$$g_m = \omega^2 C_{IN}C_{OUT} R_S \left(1 + \frac{C_O}{C_L}\right)^2$$

R_S = series resistance of the crystal
f = frequency of the crystal
Δf = frequency shift from series resonance frequency
C_O = static capacitance of the crystal
C_{IN} = input capacitance
C_{OUT} = output capacitance
C_L = load capacitance
C_m = motional capacitance
$\omega = 2\pi f$

The resulting g_m should not exceed 50 μmhos

ICM7045
CMOS Precision Decade Timers

FEATURES

- **Total integration: includes oscillator, divider, decoder driver on chip**
- **Wide operating supply range: 2.5V ≤ V+ ≤ 4.5V**
- **Low operating power consumption: 0.9 mW @ 3.6V supply with display off**
- **High output current drive: 18 mA peak current per segment with 12.5% duty cycle.**
- **Leading zero suppression: timer stopwatch applications**
- **Fractional second suppression: 24-hour clock application**
- **Short duration short circuit protection on all inputs and outputs at 3.6V supply**
- **Versatility of applications: precision timer, 4 mode stopwatch, 24-hour clock**
- **Uses 6.5536 MHz quartz crystal for high accuracy**

GENERAL DESCRIPTION

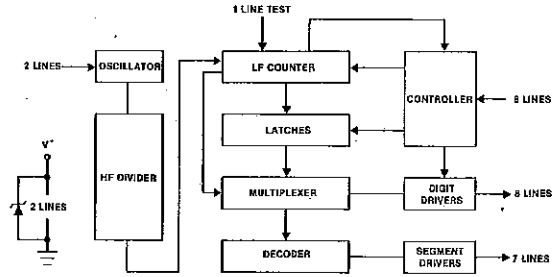
The ICM7045 is a fully integrated precision decade timer fabricated using Intersil's low voltage metal gate C-MOS technology. The oscillator, frequency divider, multiplexer, decoder, segment and digit output buffers are all included on-chip. The circuits are designed to interface directly with fully multiplexed 8-digit 7-segment common cathode LED displays. The normal supply voltage is 3.6V, equivalent to a stack of three nickel cadmium batteries.

This circuit is designed for use as a digital timer, 4-function stopwatch and 24 hour clock; the only external components required are the display, batteries, 6.5536 MHz crystal, turning capacitor and 4 switches.

The ICM7045 divides the oscillator frequency in sixteen binary stages to a frequency of 100 Hz; some of these intermediate outputs are used to generate the multiplex waveforms at a 12.5% duty cycle/800 Hz rate. The 100 Hz signal is then processed in the counters and multiplexed in the decoders.

7

BLOCK DIAGRAM



ZENER DIODE HAS TYPICAL BREAKDOWN VOLTAGE OF 5.6V

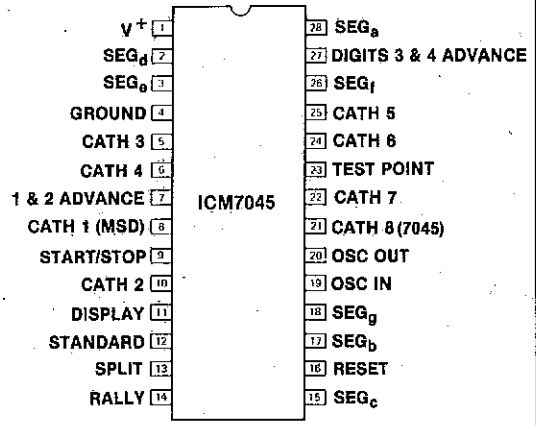
ORDERING INFORMATION

ICM7045 I DI

Package
28 Pin Plastic DIP
Temperature Range
I = Industrial −20°C to +85°C
Type

Order Dice by Following Part Number — ICM7045/D

PIN CONFIGURATION (outline dwg DI)



ABSOLUTE MAXIMUM RATINGS

Power Dissipation (1) 1W
Supply Voltage ..... +5.5V
Input Voltage ..... Equal to, but never in excess of the supply voltages
Output Voltage ..... Equal to, but never in excess of the supply voltages
Digit Drive Output Current 150mA/digit
Storage Temperatures ..... −55°C to +125°C
Operating Temperatures ..... −20°C to +85°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This value of power dissipation refers to that of the package and will not be obtained under normal operating conditions.

TYPICAL OPERATING CHARACTERISTICS

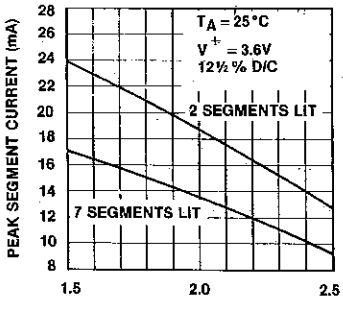
TEST CONDITIONS: $V+ = 3.6V$, $T_A = 25°C$ Parameters listed are absolute value

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I^+	Display Off		180	2000	µA
		7 Segments Lit $V_F = 1.8V$	70	105		mA
		2 Segments Lit $V_F = 1.8V$	28	42		mA
Operating Voltage	V^+	$-20°C < T_A < 85°C$	2.5		4.5	V
Segment Current Drive	I_{SEG}	7 Segments I.T., $V_F = 1.8V$, 12.5% Duty Cycle				
Instantaneous			10	15		mA
Average			1.25	1.825		mA
Segment Current Drive		2 Segments Lit, $V_F = 1.8V$ 12.5% Duty Cycle				
Instantaneous			14	21		mA
Average			1.75	2.625		mA
Min. Switch Actuation Current, Any Switch	I_{SW}		50			µA
Digit Driver Leakage Current	I_{DLK}				200	µA
Segment Driver Leakage Current	I_{SLK}				200	µA
Typical Oscillator Stability	f_{STAB}	$3V \le V^+ \le 4V$, $C_{TUNING} = 15pF$		1.0		ppm
Oscillator Start Up Time	t_{start}	$V^+ = 3.6V$			0.1	sec
		$V^+ = 2.5V$			1.0	sec
Oscillator Input Capacitance	C_{IN}			17		pF

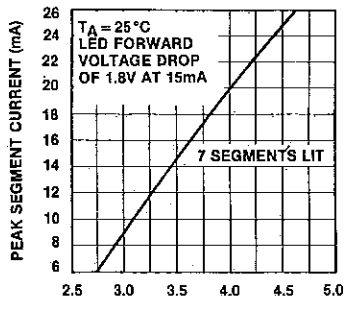
7

TYPICAL PERFORMANCE CURVES

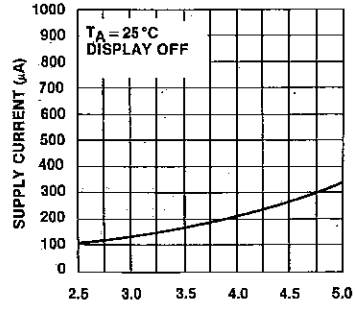
PEAK SEGMENT CURRENT DRIVE VS. LED SEGMENT VOLTAGE DROP



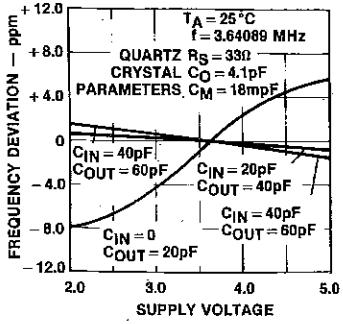
PEAK SEGMENT CURRENT VS. SUPPLY VOLTAGE

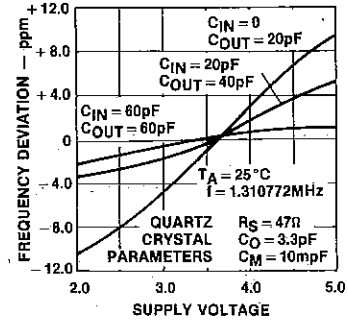


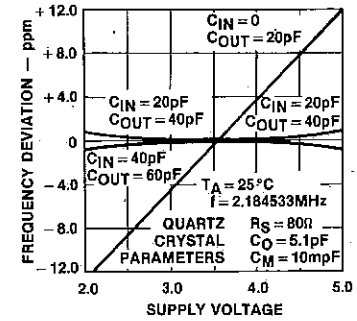
SUPPLY CURRENT VS. SUPPLY VOLTAGE



OSCILLATOR STABILITY VS. SUPPLY VOLTAGE FOR 3 DIFFERENT QUARTZ CRYSTALS



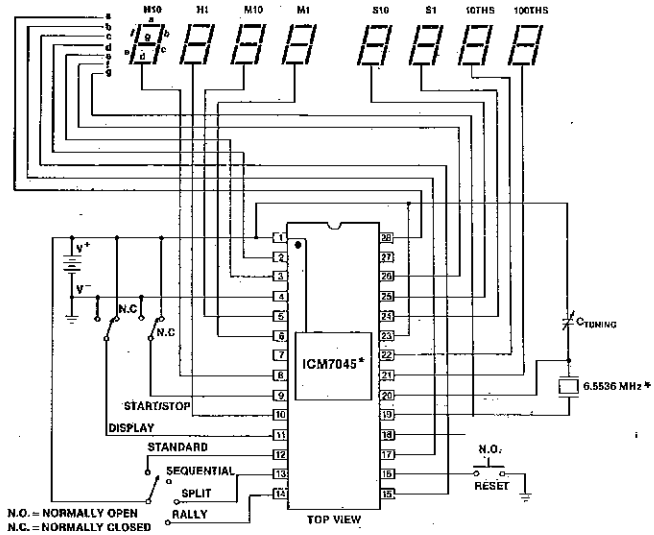




ICM7045

7

Quartz Crystal Parameters
f = 6.5536 MHz
$R_S = 40Ω$
$C_1 = 15mpF$
$C_O = 3.5pF$



NOTE: Specify quartz crystal to have nominal frequency value when tuned by a total parallel capacitance value of 12 pF or less.

Figure 1: Four Stopwatch Modes

FUNCTIONAL OPERATION

STOPWATCH/TIMER OPERATION

The control inputs used in the complete stopwatch application are: (refer to fig. 1)

START/STOP	RESET	SPLIT
DISPLAY	STANDARD	RALLY

START/STOP and DISPLAY are designed for connection to single pole double throw switches to insure operation free of contact bounce.

The switch connected to RESET can be normally open single pole single throw. STANDARD, SPLIT and RALLY are control points with internal pull down resistors to V^-. These are designed to be connected to a rotary function switch which will connect no more than one of these points to V^+. If STANDARD (SPLIT, RALLY) is connected to V^+ the stopwatch is said to be in the STANDARD (SPLIT, RALLY) mode. If all three are left open, the stopwatch is in the SEQUENTIAL mode.

RESET FUNCTION

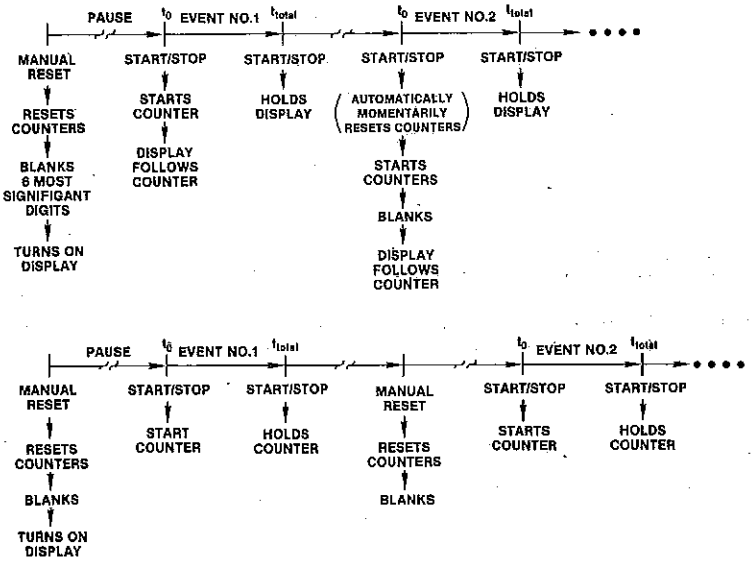
When the stopwatch is turned on, the RESET will normally be activated. This puts the stopwatch in a ready condition by:

1. Resetting all circuitry
2. Blanking seconds, minutes, hours
3. Showing 00 in the two least significant digits.
4. Turning on the display if it was previously turned off

The display of just two zeros in the two least significant digits gives the complete assurance that the stopwatch is "ready to go".

STANDARD MODE

In the STANDARD mode, after a reset has taken place, START/STOP is activated at time t_0. The clock and display are moving simultaneously. A second activation of START/STOP stops the clock and holds the display at time t_{total}. This completes an event. For timing a second event there are two options. One is to activate START/STOP at the start of the second event. This will momentarily reset the counter and display so that the timing of the second event proceeds from zero. Another activation of START/STOP stops the counter and display at time t_{total} to end the second event. The other option is to activate RESET after the first event is over. Then the second event proceeeds similarly to the first event. As is clear from this description, RESET can be used at any time to reset the stopwatch, including when a timing is in progress. The DISPLAY input can be activated to turn the display off and on. If the display is off when RESET is activated, it will reset and turn on. Turning off the display for timing long events will result in a very substantial power saving.

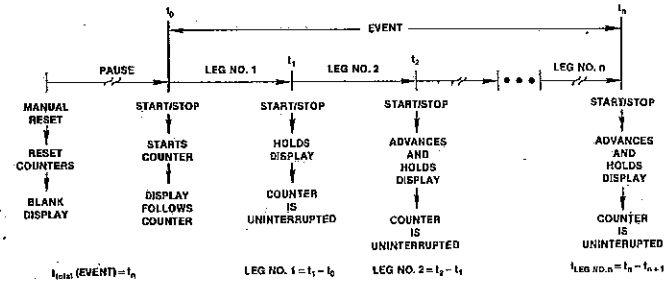


SEQUENTIAL MODE

The sequential mode of the stopwatch is designed for timing events consisting of more than one leg (such as relays, multilap races, etc.). After the initial reset the START/STOP is activated at t_0 to start the event. A second activation of START/STOP at time t_1 stops the display and allows t_1 to be read out, while the clock resets and starts counting again instantaneously. At time t_2 an activation of START/STOP enters t_2 (the time of leg 2) into the display. This sequence can continue indefinitely. Assuming the total event has n legs, the total elapsed time is then equal to the sum of the n times read out:

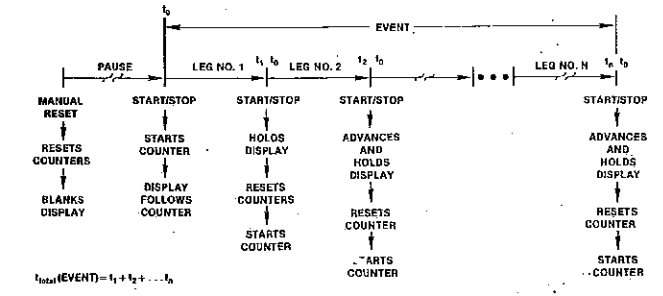
$$t_{total} = t_1 + t_2 \ldots + t_n$$

If it is desired to see the moving clock after a time has been recorded, the DISPLAY switch can be activated to release the display hold and catch up with the moving clock. The display cannot be turned off in the sequential mode. RESET can be activated at any time to reset clock and display.



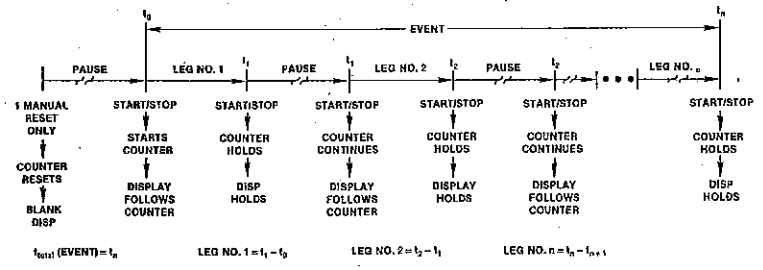
SPLIT MODE

The split mode is another mode for timing multileg events. In contrast to the sequential mode, the timing in the split mode is cumulative. From a reset condition, the START/STOP switch is activated at t_0 to start the counter and display running. A second activation at t_1 stops the display and allows t_1 to be read out while counter continues timing. A third activation at t_2 advances the display with the total elapsed time from t_0 to t_2 showing. Finally, at time t_n the total elapsed time of the event is entered in the display. The time of one leg of the event can be obtained by subtraction. The display can be synchronized to the counter (catch-up function) at any time by activating the display switch. To reset the timer, activate reset. The display cannot be turned off in the SPLIT mode.



RALLY MODE

The rally mode is designed for timing of events with interruptions. Consider an n leg event where the legs may be separated by intervals which should not be timed. The rally mode starts with a RESET. At time t_0 the stopwatch is started by activating START/STOP. After this point the RESET function is disabled to prevent accidental resets during long timing intervals. At time t_1 a START/STOP pulse stops counter and display. From here on each leg time is added to the total by a START/STOP pulse at the beginning of the leg and at the end. The individual leg times are determined by subtraction. The display can be turned on and off with the display switch.



CLOCK OPERATION

The control inputs used in a possible 24-hour clock configuration are (refer to fig. 2):

START/STOP
MINUTES ADVANCE
HOURS ADVANCE
RALLY

START/STOP, MINUTES ADVANCE and HOURS ADVANCE are designed for connection to single pole double throw switches; this assures contact bounce elimination on these inputs. To avoid an additional switch for the DISPLAY input, the RALLY input should be connected to V^+ through a 20k resistor and to V^- through a 0.01μF capacitor. These components insure that the display is on when power is applied to the circuit. The most convenient setting procedure is:

1. If clock is not running when power is applied activate START/STOP switch.
2. Depress MINUTES ADVANCE switch to obtain correct minutes setting, one minute count per activation.
3. Depress HOURS ADVANCE switch to obtain correct HOURS setting, one hour count per activation.

It is possible to set the clock more accurately or to correct small time errors by using START/STOP in combination with MINUTES ADVANCE. If the clock is, for instance, 20 seconds slow, activate the MINUTES ADVANCE once, then activate the START/STOP, wait 40 seconds and activate the START/STOP again. If the clock is 20 seconds fast, the START/STOP switch should be activated to stop the clock, then after 20 seconds activated again to restart the clock. Other clock configurations are possible (see Application Notes).

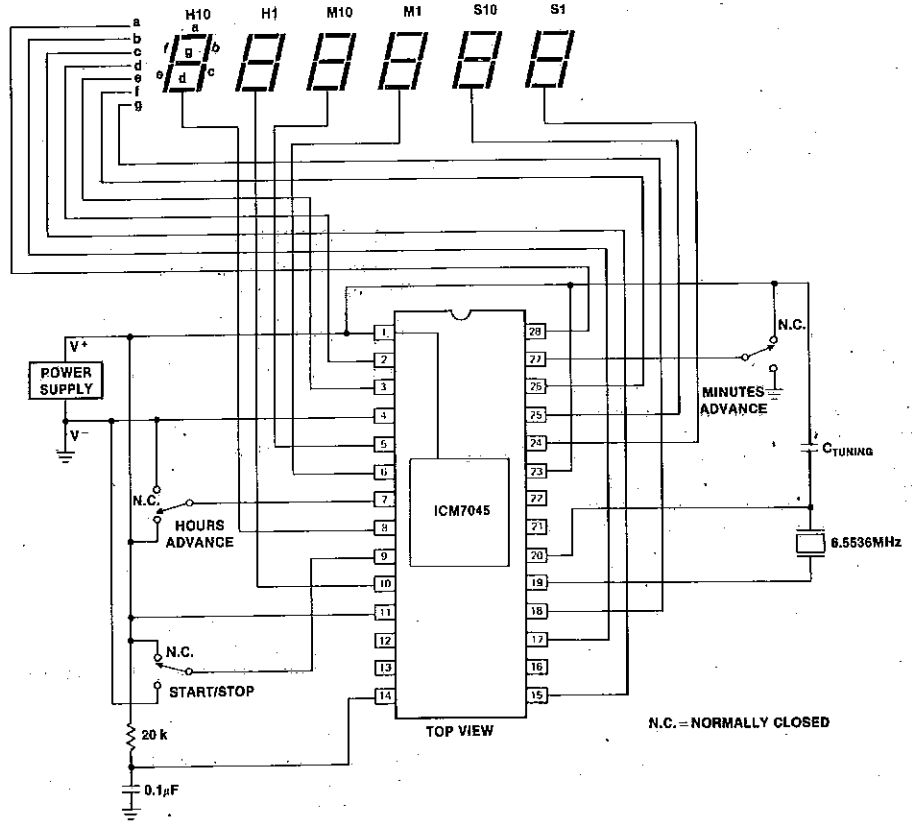


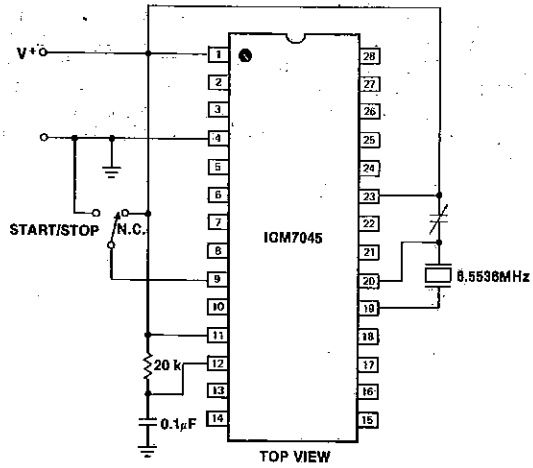
Figure 2: Clock Mode

APPLICATION NOTES

The ICM7045 have been designed with versatility of applications in the digital timer/stopwatch/24-hour clock field as the major objective. The simplicity of operating modes allow for an extremely practical, easy to use stopwatch, at the same time permit the design of a variety of simple lapse timer, stopwatch and clock circuits; a few of these will be shown and discussed briefly here.

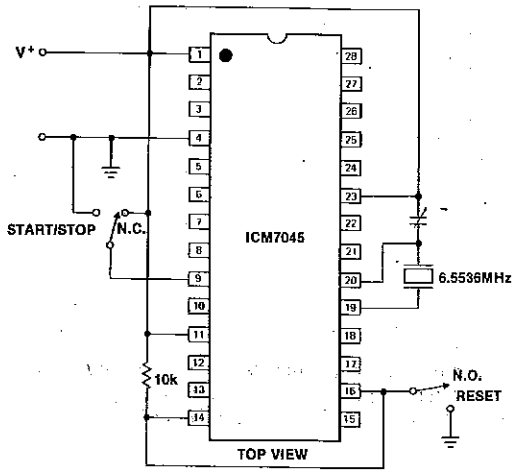
TIMER CIRCUIT I

This simple circuit (display connections not shown) allows interval timing up to 24 hours with a resolution of 0.01 second. Each interval is timed by one start and one stop pulse on the start/stop line. The start pulse for the next interval to be timed automatically resets the timer. Leading zero suppression is automatic.



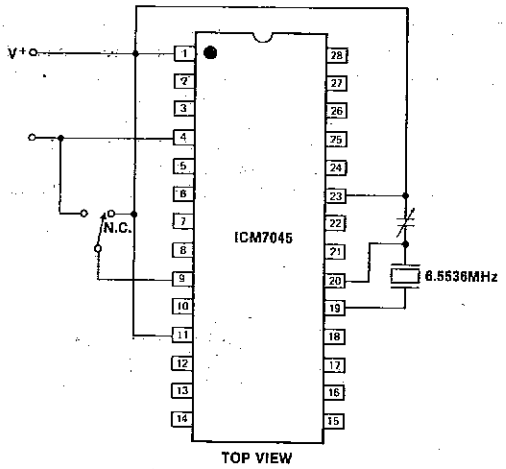
TIMER CIRCUIT II

This circuit allows cumulative timing of intervals. Each interval is timed by one start and one stop pulse on the start/stop line. Each subsequent interval timed adds to the total line displayed. The reset switch allows the timer to be reset to zero to start another sequence of intervals. Note that the time between the end of one interval and the start of the reset is not recorded nor added to the total.



TIMER CIRCUIT III

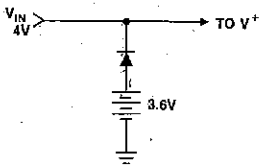
This circuit allows interval timing with a single pulse on the start/stop line. Each pulse enters the time elapsed since the previous pulse into the display, resets the timer and starts the timer for the next interval.



CLOCK CIRCUIT I

The standard clock circuit is shown and described in fig. 2. The clock accuracy with a stable voltage supply will depend mostly on the temperature and aging characteristics of the crystal.

The power supply can be modified to give battery standby power.

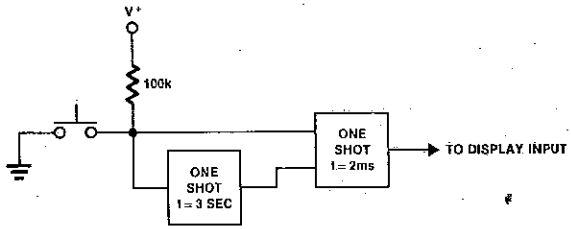


The standby circuit should be designed to provide the specified minimum voltage to the ICM7045.

OTHER CLOCK CIRCUITS

The basic clock circuit can be modified for various special applications. If it is desired to turn the display on and off, then connect the display input to an additional SPDT switch, while omitting the capacitor/resistor combination on the STANDARD input.

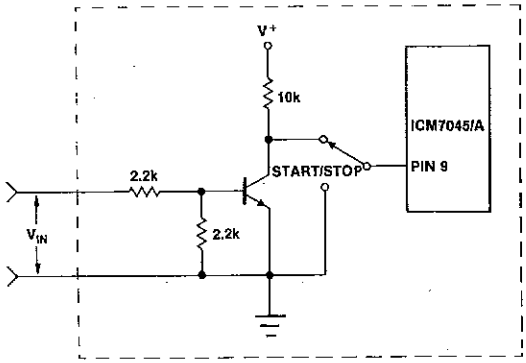
This input can then be wired directly to V^+. This 24-hour clock version might be applicable to vehicles, boats, etc. where a battery is available to supply the display off clock current, while the display can be turned on with the ignition. Another possible configuration would connect a special circuit to the DISPLAY input which generates a double pulse about 3 seconds apart:



This means depressing the switch will turn on the clock's display for 3 seconds. This allows design of a battery operated "on demand" digital 24-clock.

STOPWATCH EXTERNAL SYNC CIRCUIT

If the stopwatch is connected as shown in fig.1, a few additional components will allow external synchronization of the stopwatch in any mode:



NOTE: Be sure to minimize the distance between the transistor and the ICM7045 to prevent noise from being generated along this connection. *Noise spikes absolutely must not exceed the supply voltages.*

The external sync signal source must supply a positive pulse to activate the START/STOP input. The minimum voltage of this pulse is about 1.2V in the circuit as shown, but the triggering level can be changed by modifying the input resistor ratio. The output impedance of the external sync signal source should be no greater than 4k ohms.

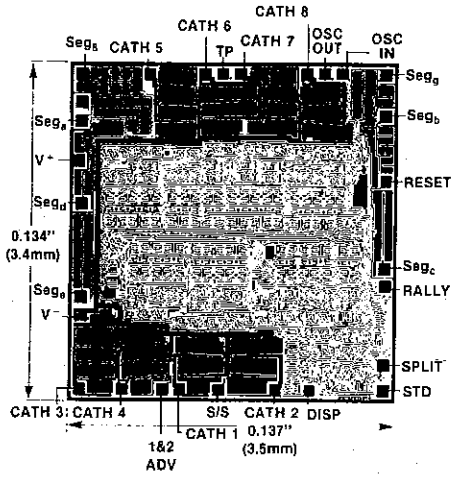
OSCILLATOR CONSIDERATIONS

The oscillator is a high gain complementary MOS inverter with on-chip feedback resistors and an on-chip fixed input capacitor of 22pF. For the 6.5536 MHz crystal needed for normal timing using the ICM7045, it is suggested that the nominal load capacitance be kept under 12pF to keep total loading on the oscillator to a reasonable level. The actual trimmer range and the nominal load capacitance needed will have to be determined from the total stray capacitance of the particular circuit (including ICM7045 with package, PC board, etc.) and the tuning tolerance of the chosen crystal.

The series resistance of the crystal should also be kept to a low value (typically less than 50 ohms) to achieve adequate low voltage operation.

Oscillator tune up can be most easily performed using a pull-up resistor of 10k ohms on the fractional seconds digit, using period average tune for 1.25ms (800Hz).

CHIP TOPOGRAPHY



7

ICM7050
ICM1115
Quartz Clock Circuits
Bipolar Stepper Motor Applications

FEATURES

- Single battery operation
- Very low current - typically 40μA at 4.19MHz
- Reset or stop function, inhibited during output
- Extremely low output saturation resistance: less than 100 ohms
- Complex direct drive alarm: 1Hz + 8Hz + 2048Hz
- Custom options available

ORDERING INFORMATION

DEVICE	MOTOR OUTPUT	ALARM OUTPUT
ICM7050	47ms @ 0.5 Hz	Complex
ICM1115	0.5 Hz Square Wave	64 Hz Tone

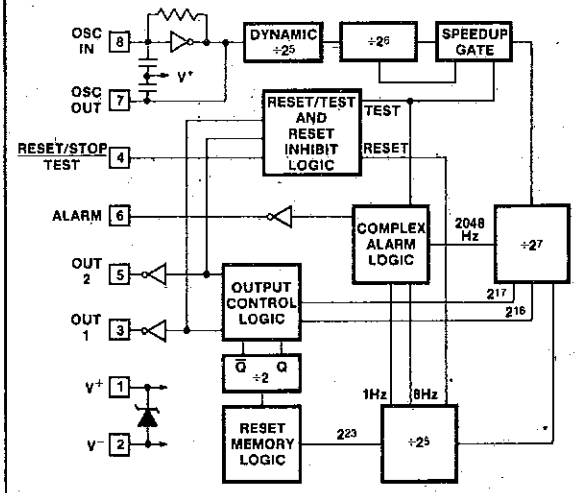
Note: These devices require a crystal frequency of 4.19 MHz. Consult ICM7070 data sheet for 32.768 kHz devices.

*See **PART NUMBER CHANGES** below.

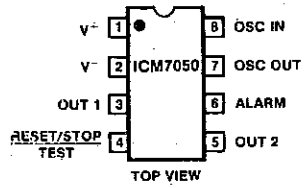
GENERAL DESCRIPTION

The ICM7050/ICM1115 are single battery analog quartz clock circuits intended for use with bipolar stepper motors and fabricated using Intersil's low voltage metal gate CMOS process, The circuits consist of a divider chain, output gating, output buffers and an oscillator which, when using the specified 4.19MHz crystal and capacitors, provides excellent stability. The high frequency portion of the divider chain consists of dynamic dividers, while the remainder are static. The dynamic dividers feature low power consumption and operating voltage, but limit low frequency operation. The 2^{23} divider chain is tapped at the 2^{11}, 2^{19}, and 2^{22} points to provide a complex alarm of 1Hz, 8Hz, and 2048Hz driving an output inverter. Several standard motor drive waveforms are available, and the large output inverters provide the low impedance necessary to drive the motor. A reset inhibit function is provided so that if the RESET occurs during an output pulse, resetting will not take place until the pulse is completed. RESET may also be used as a stop for synchronization to a time signal or tester. Motor drive will continue 1 sec. after RESET is released.

BLOCK DIAGRAM

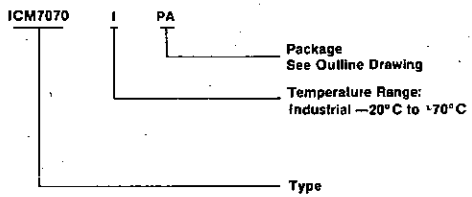


PIN CONFIGURATION (outline dwg PA)



TOP VIEW

ORDERING INFORMATION



Order Devices by Following Part Number — ICM7050IPA
ICM1115AIPA
ICM1115BIPA

CUSTOM OPTIONS

The ICM7050 input and output configurations may be customized for:

- On-chip oscillator capacitance up to 20 pF at OSC IN or OSC OUT
- Output pulse frequency from 0.5 Hz to 64 Hz (standard crystal freq.)
- Output pulse width from 0.98 msec to 50% duty cycle
- Alarm output up to three binary frequencies from 1 Hz to 2048 Hz

Consult factory for mask programming charge and minimum order requirements.

7

ABSOLUTE MAXIMUM RATINGS

Power Dissipation Output Short Circuit (Note 1)	300mW
Supply Voltage	3V
Output Voltage (Note 2)	Equal to but never
Input Voltage (Note 2)	exceeding the supply voltage
Storage Temperature	−30°C to +125°C
Operating Temperature	−20°C to +70°C
Lead Temperature (soldering, 10s)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: This value of power dissipation refers to that of the package and will not normally be obtained under normal operating conditions.

NOTE 2: Due to the inherent SCR structure of junction isolated CMOS devices, the circuit can be put in a latchup mode if large currents are injected into device inputs or outputs. For this reason special care should be taken in a system with multiple power supplies to prevent voltages being applied to inputs and/or outputs before power is applied. If only inputs are affected, latchup can also be prevented by limiting the current into the input terminal to less than 1mA.

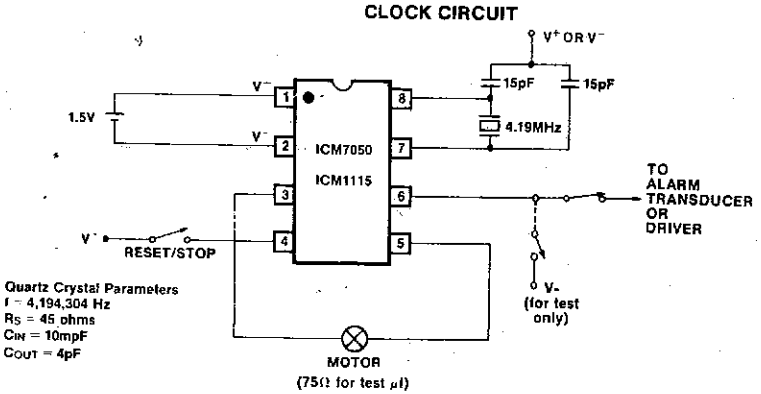
ELECTRICAL CHARACTERISTICS

($V+ = 1.5V$, $f_{osc} = 4,194,304Hz$ test circuit, $T_A = 25°C$, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current(Note 3) except ICM1115A	I^+	No Load		40	60	μA
ICM1115A Only				80	120	
Operating Voltage	V^+	$-20°C < T_A < 70°C$	1.2		1.8	V
Total Output Saturation Resistance	R_{OUT}	$I_L = 4mA$		70	100	Ω
Alarm Saturation Resistance	$R_{AL(on)}$	P, $I_L = 1mA$		400	700	Ω
		N, $I_L = 2mA$		100	400	Ω
Oscillator Stability	f_{stab}	$1.2 \le V^+ \le 1.6$		1		ppm
Oscillator Start-up Time	t_{start}	$V^+ = 1.2V$			1.0	sec
Oscillator Transconductance (Note 3)	g_m	ICM7050	75	200		μmho
		ICM1115A	150	400		
		ICM1115B	75	200		

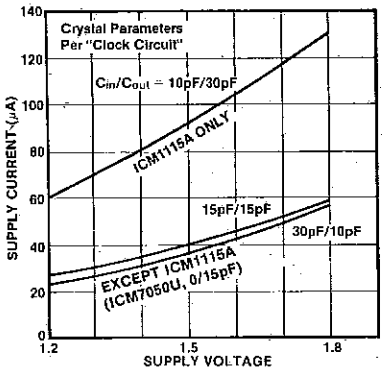
NOTE 3: Two options are available with the ICM1115. The ICM1115B is designed to be used with crystals whose load capacitance is 12 pF or less. Using input and output capacitors of 15 to 20 pF, this device will provide stable operation at very low supply current. For applications with larger load capacitance (15 to 20 pF), the ICM1115A ensures that an increased oscillator current is available to guarantee startup and operation over the voltage range. Using input and output capacitors of 30 to 40 pF, the ICM1115A will offer good stability at a supply current approximately twice that of the ICM1115B.

TYPICAL APPLICATION (also TEST CIRCUIT)

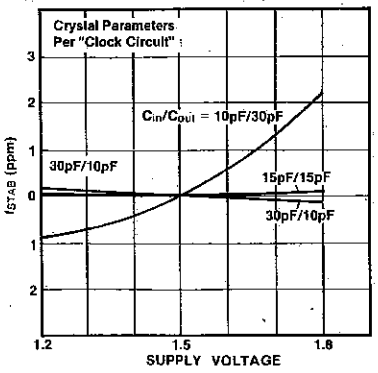


TYPICAL OPERATION CHARACTERISTICS

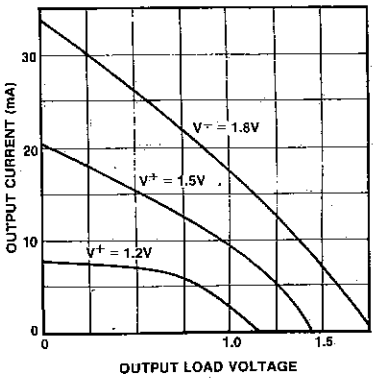
SUPPLY CURRENT vs SUPPLY VOLTAGE



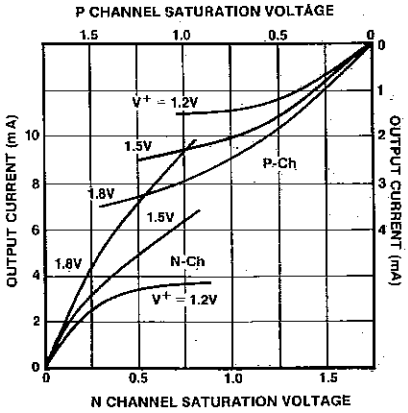
OSCILLATOR STABILITY vs. SUPPLY VOLTAGE



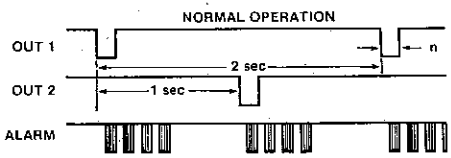
OUTPUT CURRENT vs OUTPUT LOAD VOLTAGE



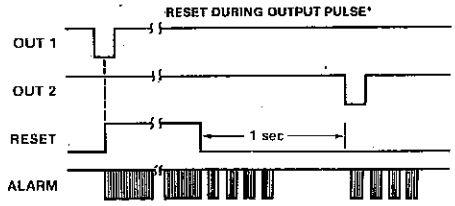
ALARM OUTPUT CURRENT vs SATURATION VOLTAGE



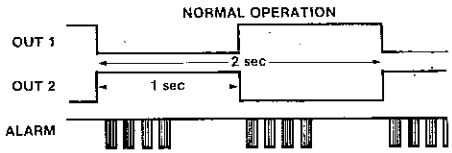
OUTPUT WAVEFORMS (ICM7050)

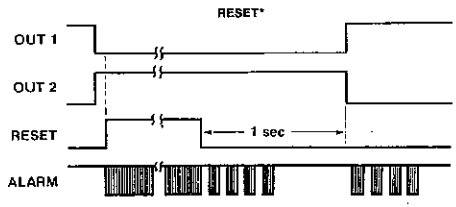


n = 47 msec for ICM7050



OUTPUT WAVEFORMS (ICM1115)





*Shown during OUTput 1; exchange OUTput 1 and OUTput 2 for opposite case.

APPLICATION NOTES

OSCILLATOR CONSIDERATIONS

The oscillator of the ICM7050 has been designed to operate with crystals having a load capacitance of 10 to 12pF. This allows nominal capacitor values of 15/15pF or 20/20pF. Increasing the load capacitance of the crystal requires larger oscillator device sizes, which causes the supply current to increase. Modifications to the oscillator can be made on a custom basis. The tuning range can be increased by using crystals with lower load capacitances, however the stability may decrease somewhat. This can be counteracted by reducing the motional capacitance of the crystal. A non-linear feedback resistor having a maximum value at start up is provided on chip. Oscillator tuning should be done at the OSCillator OUTput.

The following expressions can be used to arrive at a crystal specification:

Tuning Range

$$\frac{\Delta f}{f} = \frac{C_m}{2(C_o + C_L)} \qquad C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}}$$

g_m required for startup

$$g_m = \omega^2 C_{in}C_{out}R_S \left(1 + \frac{C_o}{C_L}\right)^2$$

R_S = series resistance of the crystal
f = frequency of the crystal
Δf = frequency shift from series resonance frequency
C_o = static capacitance of the crystal
C_{in} = input capacitance
C_{out} = output capacitance
C_m = motional capacitance
$\omega = 2\pi f$

The resulting g_m should not exceed 50μmhos.

OSCILLATOR TUNING METHODS

When tuning the oscillator two methods can be used. The first method would be to monitor the output pulse at either OUT 1 or OUT2 with a counter set to measure the period. The oscillator trimmer would then be adjusted for a reading of 2.000000 secs. A second method would be to put the device in the **reset** mode by pulling the RESET pin to V_+ and then monitor the ALARM output with a counter set to measure average period. The ALARM output is a continuous 2048Hz when in the **reset** mode, which gives a period of 488.28125μs.

The trimmer capacitor used for tuning should be connected to the OSCillator OUTput. Otherwise, if tuned at the input, the stability will vary with tuning, and the current drain may become excessive when the input capacitance is much less than the output capacitance. Refer to the Supply Current vs. Supply Voltage and Oscillator Stability vs. Supply Voltage characteristic curves on the preceding page.

TEST MODE OPERATION

Pulling the RESET/TEST input to —7V switches the device into the **test** mode to speedup automatic testing. When in the **test** mode the output rate is increased 16 times, from 1Hz to 16Hz, with a corresponding reduction in pulse width. The ALARM output changes to a composite waveform of 16Hz and 128Hz. The circuit can be **reset** while in the **test** mode by shorting the ALARM output to V^-.

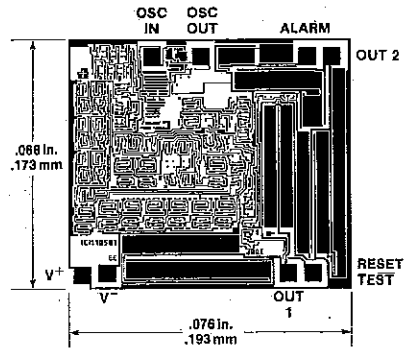
ALARM CONSIDERATIONS

The ALARM output inverter is large enough to directly drive transducers requiring up to 2mA of current. If more current is needed, a PNP buffer should be used*. A slight flutuation in the supply current of 0.5μA to 1.0μA will be seen; this is a result of 2048Hz driving the relatively large gate capacitance of the alarm output transistors.

*See Intersil Application Bulletin A031 for details.

7

CHIP TOPOGRAPHY



ICM7051
CMOS Auto Clock Circuit

FEATURES

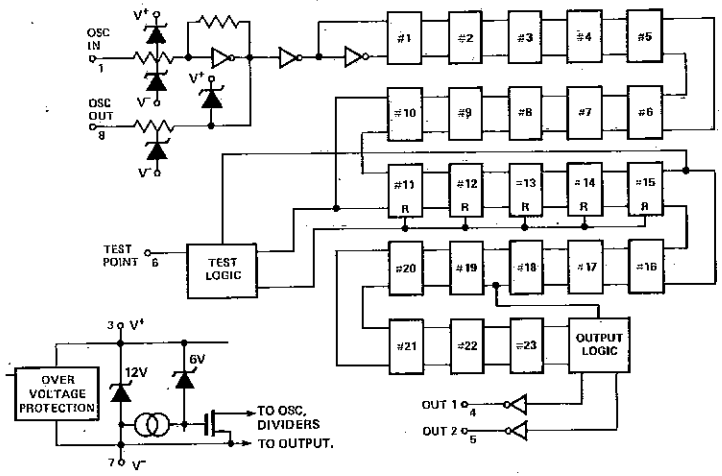
- Wide operating supply voltage and temperature ranges
- Excellent oscillator stability
- Short circuit protected bridge output with low ON resistance
- Oscillator feedback resistor on-chip
- All inputs fully protected
- Nominal 12.6 volt zener on chip
- 64Hz output for synchronous motor applications (ICM7051A)
- 1 Hz output with 31.2 ms output pulse width for stepper motor applications (ICM7051B)
- Typical power dissipation < 4 mW at 12 volts

GENERAL DESCRIPTION

The ICM7051A/B is an auto clock circuit fabricated using Intersil's standard metal gate CMOS process. Included on-chip are the oscillator, dividers, output drivers and over-voltage protection circuitry. The oscillator of the ICM7051A/B has the feedback component on-chip, and when used with the specified crystal parameters will give excellent stability. The binary dividers of the ICM7051 allow division from 4.19MHz and drive a bridge output which provides an alternating 31.2ms output pulse at 1Hz for the ICM7051B (0.5Hz each side) or a 64Hz square wave output for the ICM7051A. The bridge output consists of two large inverters with the output ON resistance of the N and P channel devices together being less than 100 ohms with V_{BATT} equal to 13.5 volts and load current equal to 10mA.

The ICM7051 series contains an on-chip zener which, when used with an external resistor and capacitor, will provide protection against over-voltage transients that may occur in an automobile environment.

SCHEMATIC DIAGRAM



ORDERING INFORMATION

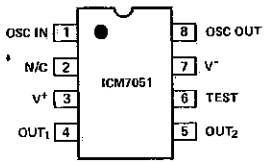
ICM7051A
ICM7051B | I | PA

- PACKAGE: PA = 8 PIN MINIDIP
- TEMPERATURE RANGE: -20°C to +85°C
- TYPE

Order dice by following part numbers: ICM7501A/D, ICM7051B/D

Note: The ICM7051A was formerly known as ITS 9042-1.

PIN CONFIGURATION (outline dwg PA)



7

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{BATT}, see TEST CIRCUIT) ..... -12 to +25V (Note 1)
..... -0.5 to +13.5V
Output Voltage and T.P. Input ..... Not to exceed supply voltage
Storage Temperature ..... -40°C to +125°C
Operating Temperature ..... -20°C to +85°C
Lead Temperature (Soldering, 10 sec) ..... 300°C
Power Dissipation (Note 2) ..... 0.5 Watt
Latch up holding current (Note 3) 100mA

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Stress duration not to exceed 2 min.
Note 2: This value of power dissipation refers to that of the package and will not be normally obtained under normal operating conditions.
Note 3: A destructive latch up mode is possible if an input or output is forward biased with respect to either the positive or negative supplies. The ICM7051 has an absolute maximum latch up holding current of 100mA. This means the device, when operated at ambient temperature, will return to its normal operating state after an inadvertant input transient, if the supply current is limited to less than the absolute maximum latch up holding current of the device.

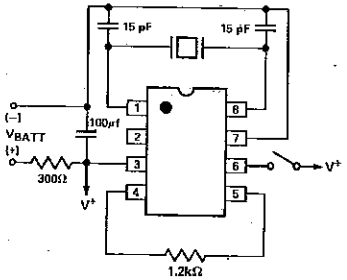
OPERATING CHARACTERISTICS

V_{BATT} = 13.5V, T_A = 25°C, f_{OSC} = 4.194304MHz, R_L = 1.2 kΩ, unless otherwise specified

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
Supply Current	I^+	No Load	V_{BATT} = 13.5V			7	mA
			V^+ = 7.0V			1	
Supply Voltage Range (Note 4)	V_{BATT}	T_A = 25°C		4.5	>3.5	22	V
		-20°C ≤ T_A ≤ +85°C		7.0		17	
Output Resistance (n+p)	R_{OUT}	I_O = 10mA				100	Ω
		V^+ = 5V, I_O = 5mA			130		
Zener Voltage	V_Z	I_Z = 5mA		11		14	V
Oscillator Stability	f_{STAB}	6V ≤ V^+ ≤ V_Z				2	ppm
Oscillator Start Up Time	t_{START}	6V ≤ V^+ ≤ V_Z				1	sec
Output Leakage Current	I_{OLK}	All Outputs				100	μA
Oscillator Transconductance	gm	V^+ ≥ 6.0V			250		μmho
		V^+ ≥ 3.0V		25	100		

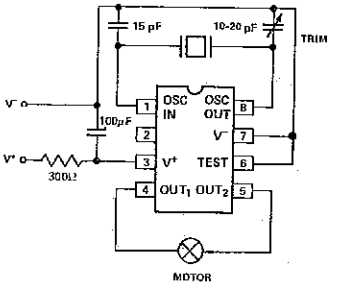
Note 4: In Test Circuit only. V^+ should not exceed V_Z.

TEST CIRCUIT



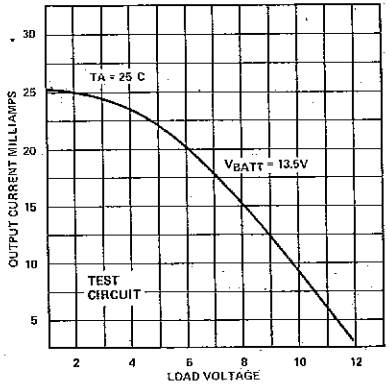
TYPICAL AUTO CLOCK

Quartz Crystal Parameters
R_S = 100Ω
C_m = 0.012 pF
C_O = 5 pF
f = 4.194,304 Hz

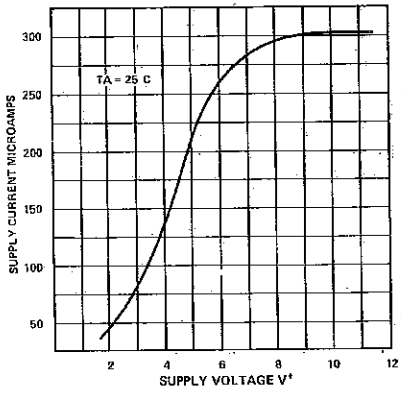


TYPICAL OPERATING CHARACTERISTICS

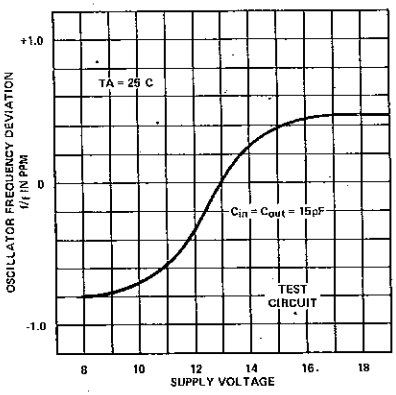
Output Current as a Function of Load Voltage



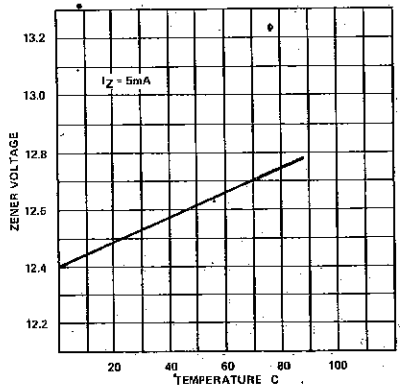
Supply Current as a Function of Supply Voltage



Oscillator Stability as a Function of Supply Voltage

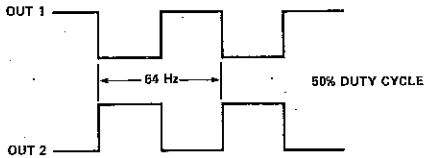


Zener Voltage as a Function of Temperature

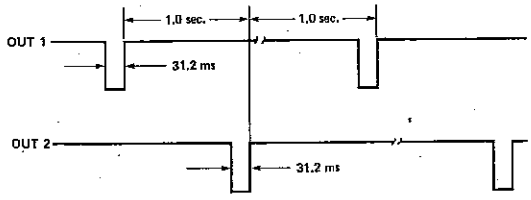


OUTPUT WAVEFORMS

ICM 7051A



ICM 7051B



The ICM7051 uses a TEST point to facilitate testing. This pin has an on-chip pulldown resistor, and for normal operation is at V^-. Connecting this pin to V^+ will give a 32 times speed-up of the outputs.

CUSTOM VERSIONS

The ICM7051 may be modified with alternative metal masks to provide a different number of dividers, various pulse widths, increased oscillator transistors or optional V zener pad for use with an external zener diode. The ICM7051 can be adapted for use with different synchronous motors as well as a variety of stepping motors. Consult factory for details.

APPLICATION NOTES

OSCILLATOR CONSIDERATIONS

The oscillator of the ICM7051 has been designed to operate with crystals having a load capacitance of 10 to 12pF. This allows nominal capacitor values of 15/15pF or 20/20pF. Increasing the load capacitance of the crystal requires larger oscillator device sizes, which causes the supply current to increase. Modifications to the oscillator can be made on a custom basis. The tuning range can be increased by using crystals with lower load capacitances, however the stability may decrease somewhat. This can be counteracted by reducing the motional capacitance of the crystal. A non-linear feedback resistor having a maximum value at start up is provided on chip.

The trimmer capacitor used for tuning should be connected to the OSCillator OUTput. Otherwise, if tuned at the input, the stability will vary with tuning, and the current drain may become excessive when the input capacitance is much less than the output capacitance. Refer to the Supply Current vs. Supply Voltage and Oscillator Stability vs. Supply Voltage characteristic curves on the preceding page.

To tune the oscillator, the best method is to monitor the output pulse at either OUT1 or OUT2 with a counter set to measure the period. The oscillator trimmer is then adjusted for a reading of 15.625 msec for the ICM7051A, or 2.0000 secs for the ICM7051B. Note that different output frequencies can be obtained by varying the crystal frequency over a range of 1 to 10MHz. In particular, a 60Hz output will result if a 3.93216MHz crystal is used with the ICM7051A.

The follwing expressions can be used to arrive at a crystal specification:

Tuning Range

$$\frac{\Delta f}{f} = \frac{C_m}{2(C_o + C_l)} \qquad C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}}$$

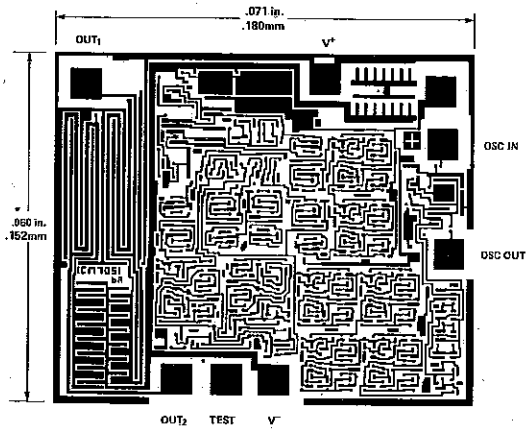
g_m required for startup

$$g_m = \omega^2 C_{in} C_{out} R_S \left(1 + \frac{C_o}{C_L}\right)^2$$

R_S = series resistance of the crystal
f = frequency of the crystal
Δf = frequency shift from series resonance frequency
C_o = static capacitance of the crystal
C_{in} = input capacitance
C_{out} = output capacitance
C_m = motional capacitance
$\omega = 2\pi f$

The resulting g_m should not exceed about 1/2 the value of the oscillator at the relevant supply voltage.

CHIP TYPOGRAPHY



7

ABSOLUTE MAXIMUM RATINGS

Power Dissipation Output Short Circuit (Note 1)	300mW
Supply Voltage	3V
Output Voltage (Note 2)	Equal to but never
Input Voltage (Note 2)	exceeding the supply voltage
Storage Temperature	−30°C to +125°C
Operating Temperature	−20°C to +70°C
Lead Temperature (soldering, 10s)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: This value of power dissipation refers to that of the package and will not normally be obtained under normal operating conditions.
NOTE 2: Due to the inherent SCR structure of junction isolated CMOS devices, the circuit can be put in a latchup mode if large currents are injected into device inputs or outputs. For this reason special care should be taken in a system with multiple power supplies to prevent voltages being applied to inputs and/or outputs before power is applied. If only inputs are affected, latchup can also be prevented by limiting the current into the input terminal to less than 1mA.

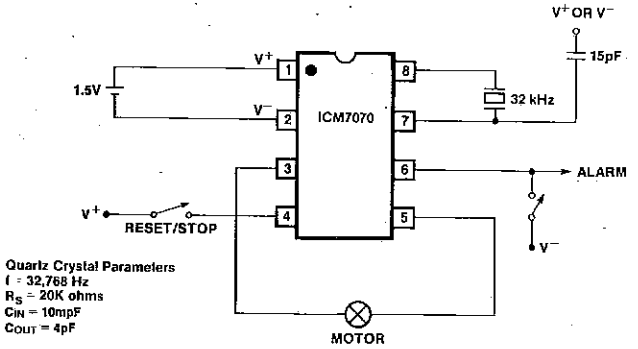
ELECTRICAL CHARACTERISTICS

($V+ = 1.5V$, fosc = 32,768 Hz test circuit, $T_A = 25°C$, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I^+	No Load		3	6	μA
Operating Voltage	V^+	$-20°C < T_A < +70°C$	1.2		1.8	V
Total Output Saturation Resistance	R_{OUT}	$I_L = 4mA$		70	100	Ω
Alarm Saturation Resistance	$R_{AL(on)}$	P, $I_L = 1mA$		400	700	Ω
		N, $I_L = 2mA$		100	400	Ω
Oscillator Stability	f_{stab}	$1.2 \le V^+ \le 1.6$		1		ppm
Oscillator Start-up Time	t_{start}	$V^+ = 1.2V$			1.0	sec
Oscillator Input Capacitance	C_{IN}		16	20	24	pF
Oscillator Transconductance	g_m		2	7		μmho

TYPICAL APPLICATION

CLOCK CIRCUIT



NOTES:

RESET/STOP: If pin 4 is not used, it should be tied to V−

OUTPUT FREQUENCIES: Crystal frequencies from 20 to 100 kHz may be used to obtain different output frequencies. See **Oscillator Considerations** for suitable crystal parameters.

ABSOLUTE MAXIMUM RATINGS

Power Dissipation Output Short Circuit (Note 1)	300mW
Supply Voltage	3V
Output Voltage (Note 2)	Equal to but never
Input Voltage (Note 2)	exceeding the supply voltage
Storage Temperature	−30°C to +125°C
Operating Temperature	−20°C to +70°C
Lead Temperature (soldering, 10s)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: This value of power dissipation refers to that of the package and will not normally be obtained under normal operating conditions.
NOTE 2: Due to the inherent SCR structure of junction isolated CMOS devices, the circuit can be put in a latchup mode if large currents are injected into device inputs or outputs. For this reason special care should be taken in a system with multiple power supplies to prevent voltages being applied to inputs and/or outputs before power is applied. If only inputs are affected, latchup can also be prevented by limiting the current into the input terminal to less than 1mA.

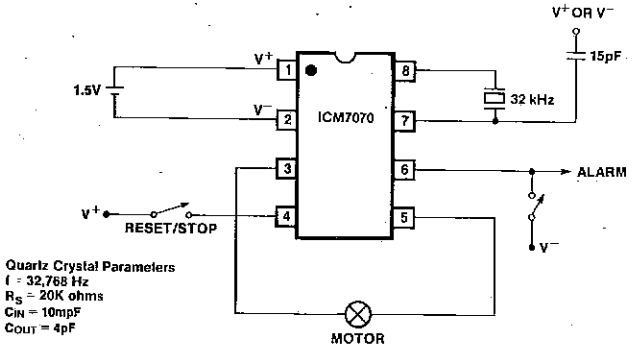
ELECTRICAL CHARACTERISTICS

($V+ = 1.5V$, fosc = 32,768 Hz test circuit, $T_A = 25°C$, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I^+	No Load		3	6	μA
Operating Voltage	V^+	$-20°C < T_A < +70°C$	1.2		1.8	V
Total Output Saturation Resistance	R_{OUT}	$I_L = 4mA$		70	100	Ω
Alarm Saturation Resistance	$R_{AL(on)}$	P, $I_L = 1mA$		400	700	Ω
		N, $I_L = 2mA$		100	400	Ω
Oscillator Stability	f_{stab}	$1.2 \le V^+ \le 1.6$		1		ppm
Oscillator Start-up Time	t_{start}	$V^+ = 1.2V$			1.0	sec
Oscillator Input Capacitance	C_{IN}		16	20	24	pF
Oscillator Transconductance	g_m		2	7		μmho

TYPICAL APPLICATION

CLOCK CIRCUIT



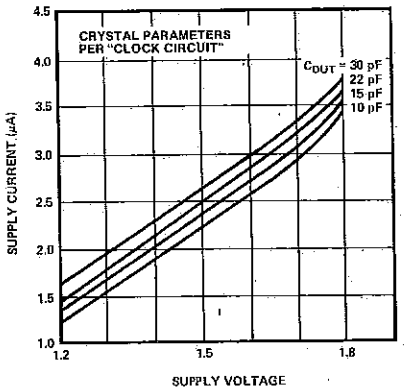
NOTES:

RESET/STOP: If pin 4 is not used, it should be tied to V−

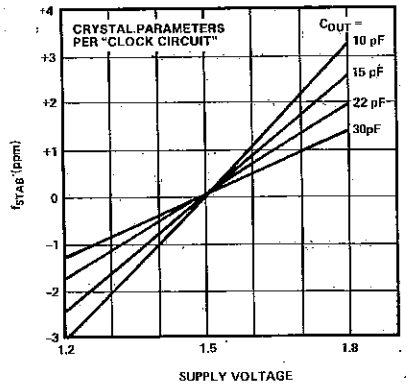
OUTPUT FREQUENCIES: Crystal frequencies from 20 to 100 kHz may be used to obtain different output frequencies. See **Oscillator Considerations** for suitable crystal parameters.

TYPICAL OPERATION CHARACTERISTICS

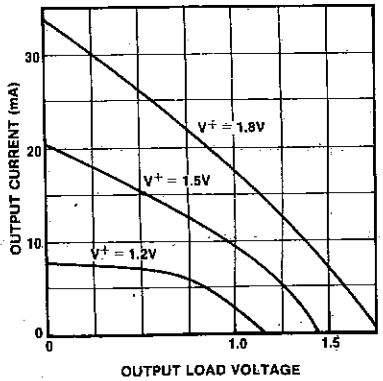
SUPPLY CURRENT vs SUPPLY VOLTAGE



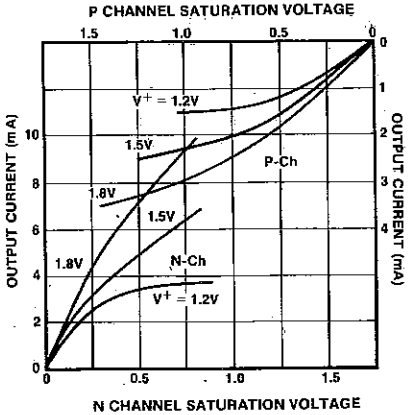
OSCILLATOR STABILITY vs. SUPPLY VOLTAGE



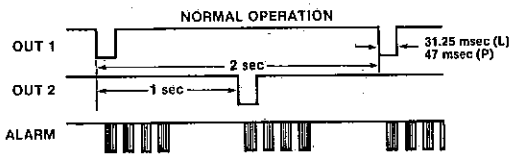
OUTPUT CURRENT vs OUTPUT LOAD VOLTAGE

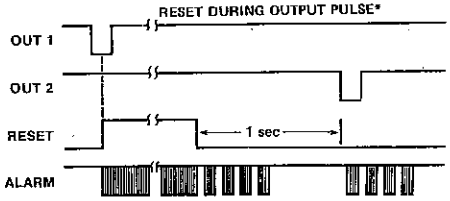


ALARM OUTPUT CURRENT vs SATURATION VOLTAGE



OUTPUT WAVEFORMS (ICM7070L)





APPLICATION NOTES

OSCILLATOR CONSIDERATIONS

The oscillator of the ICM7070 has been designed to operate with crystals having a load capacitance of 10 to 12pF. This allows nominal capacitor values of 15pF or 20pF. Increasing the load capacitance of the crystal requires larger oscillator device sizes, which causes the supply current to increase. Modifications to the oscillator can be made on a custom basis. The tuning range can be increased by using crystals with lower load capacitances, however the stability may decrease somewhat. This can be counteracted by reducing the motional capacitance of the crystal. A non-linear feedback resistor having a maximum value at start up is provided on chip. Oscillator tuning should be done at the oscillator output.

The following expressions can be used to arrive at a crystal specification:

Tuning Range

$$\frac{\Delta f}{f} = \frac{C_m}{2(C_o + C_L)} \qquad C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}}$$

g_m required for startup

$$g_m = \omega^2 C_{in}C_{out}R_S \left(1 + \frac{C_o}{C_L}\right)^2$$

R_S = series resistance of the crystal
f = frequency of the crystal
Δf = frequency shift from series resonance frequency
C_o = static capacitance of the crystal
C_{in} = input capacitance
C_{out} = output capacitance
C_m = motional capacitance
$\omega = 2\pi f$

The resulting g_m should not exceed 20 μmhos.

OSCILLATOR TUNING METHODS

When tuning the oscillator two methods can be used. The first method would be to monitor the output pulse at either OUT 1 or OUT 2 with a counter set to measure the period. The oscillator trimmer would then be adjusted for a reading of 2.000000 secs. A second method would be to put the device in the **reset** mode by pulling the RESET pin to V^+ and then monitor the ALARM output with a counter set to measure average period. The ALARM output is a continuous 2048Hz when in the **reset** mode, which gives a period of 488.28125μs.

The trimmer capacitor used for tuning should be connected to the OSCillator OUTput. Otherwise, if tuned at the input, the stability will vary with tuning, and the current drain may become excessive when the input capacitance is much less than the output capacitance. Refer to the Supply Current vs. the Supply Voltage and Oscillator Stability vs. Supply Voltage characteristic curves on the preceding page.

TEST MODE OPERATION

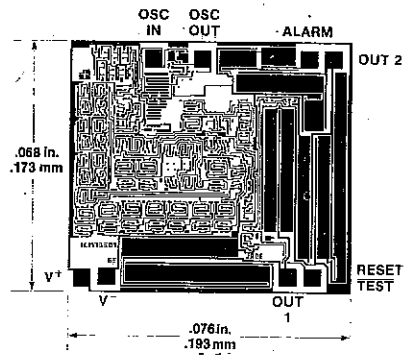
Pulling the RESET/TEST input to —7V switches the device into the **test** mode to speed up automatic testing. When in the **test** mode the output rate is increased 4 times, from 0.5Hz to 2Hz, with a corresponding reduction in pulse width. The ALARM output changes to a composite waveform of 4Hz and 32Hz. The circuit can be reset while in the **test** mode by shorting the ALARM output to V^-.

ALARM CONSIDERATIONS

The ALARM output inverter is large enough to directly drive transducers requiring up to 2mA of current. If more current is needed, a PNP buffer should be used*. A slight fluctuation in the supply current of 0.5μA to 1.0μA will be seen; this is a result of the 2048Hz drive to the relatively large gate capacitance of the alarm output transistors.

*See Intersil Application Bulletin A031 for details.

CHIP TOPOGRAPHY



ICM7206 CMOS Touch Tone™ Encoder

FEATURES

- **Low cost system with minimum component count**
- **Fully integrated oscillator uses 3.58 MHz color TV crystal**
- **High current bipolar output driver**
- **Low output harmonic distortion**
- **Wide operating supply voltage range: 3 to 6 volts**
- **Uses inexpensive single contact per key calculator type keyboard (ICM7206/C/D)**
- **Extremely low power ≤ 5.5mW with a 5.5V supply**
- **Single and dual tone capabilities**
- **Multiple key lockout**
- **Disable output: provides output switch function whenever a key is pressed**
- **Custom options available**

GENERAL DESCRIPTION

The Intersil ICM7206/A/B/C/D are 2-of-8 sine wave tone encoders for use in telephone dialing systems. Each circuit contains a high frequency oscillator, two separate programmable dividers, a D/A converter, and a high level output driver.

The reference frequency is generated from a fully integrated oscillator requiring only a 3.58 MHz color TV crystal. This frequency is divided by 8 and is then gated into two divide by N counters (possible division ratios 1 through 128) which provide the correct division ratios for the upper and lower band of frequencies. The outputs from these two divide by N counters are further divided by 8 to provide the time sequencing for a 4 voltage level synthesis of each sinewave. Both sinewaves are added and buffered to a high current output driver, with provisions made for up to two external capacitors for low pass filtering, if desired. Typically, the total output harmonic distortion is 20% with no L.P. filtering and it may be reduced to typically less than 5% with filtering. The output drive level of the tone pairs will be approximately –3dBV into a 900 ohm termination. The skew between the high and low groups is typically 2.5 dB without low pass filtering.

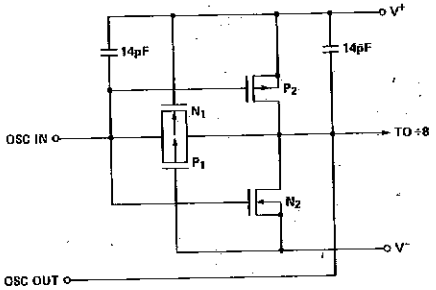
The 7206 uses either a 3 x 4 or 4 x 4 single contact keyboard; the oscillator will run whenever the power is applied, and the DISABLE output consists of a p-channel open drain FET whose source is connected to V^+.

The 7206A can also use a 3 x 4 or 4 x 4 keyboard, but requires a double contact type with the common line tied to V^+. The oscillator will be on whenever power is applied; the DISABLE output consists of a p-channel open drain FET; its' source is connected to V^+.

The 7206B requires a 4 x 4 double contact keyboard with the common line tied to V^-. The oscillator will be on only during the time that a ROW is enabled, and the DISABLE output consists of an n-channel open drain FET with its' source tied to V^-.

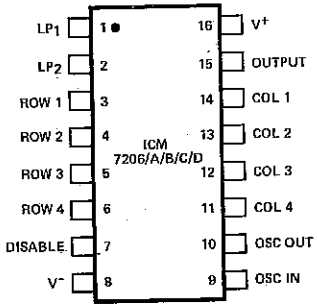
The 7206C uses either a 3 x 4 or 4 x 4 single contact keyboard; the oscillator will be on only during the time that a key is depressed. The DISABLE output consists of an n-channel open drain FET with its source tied to V^-.

The 7206D uses a single contact 3 x 4 or 4 x 4 keyboard. The oscillator will be on only during the time that a key is depressed. DISABLE output consists of a p-channel open drain FET with its source tied to V^+.



ICM7206 Oscillator

PIN CONFIGURATION (OUTLINE DRAWING PE)



Pin 1 is designated either by a dot or a notch.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7206 JPE	-40° C to +85° C	Plastic
ICM7206A JPE	-40° C to +85° C	Plastic
ICM7206B JPE	-40° C to +85° C	Plastic
ICM7206C JPE	-40° C to +85° C	Plastic
ICM7206D JPE	-40° C to +85° C	Plastic
ICM7206/D	-40° C to +85° C	DICE
ICM7206A/D	-40° C to +85° C	DICE
ICM7206B/D	-40° C to +85° C	DICE
ICM7206C/D	-40° C to +85° C	DICE
ICM7206D/D	-40° C to +85° C	DICE

7

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Note 2) 6.0V
Supply Current V^- (terminal 8) 25mA
Supply Current V^+ (terminal 16) 40mA
Disable Output Volt. (term. 7) .. Not more pos. than V^+ nor more neg. than −6V with respect to V^+
Output Volt. (term. 15). Not more pos. than +5V with respect to V^+, nor more neg. than −1.0 with respect to V^-
Output Current (terminal 15) 25mA
Power Dissipation 300mW
Operating Temperature Range ..... −40°C to +85°C
Storage Temperature Range ..... −55°C to +125°C

NOTE 1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 2. The ICM7206 family has a zener diode connected between V^+ and V^- having a breakdown voltage between 6.2 and 7.0 volts. If the currents into terminals 8 and 16 are limited to 25 and 40mA maximum respectively, the supply voltage may be increased above 6 volts to zener voltage. With no such current limiting, the supply voltage must not exceed 6 volts.

TYPICAL OPERATING CHARACTERISTICS

TEST CONDITIONS: $V^+ = 5.5V$, Test Circuit, $T_A = 25°C$ unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Supply Current	I^+	R_L disconnected			450	1000	μA
Guaranteed Operating Supply Voltage Range (Note 3)	V_{OP}	$-40°C \le T_A \le +85°C$		3.0		6.0	V
Peak to Peak Output Voltage	V_{OUT}	C_1, C_2 disconnected — Low Band		0.90	1.15	1.45	V
RMS Output Voltage		$R_L = 1k\Omega$, no filtering — High Band		1.10	1.40	1.70	V
		$R_L = 1k\Omega$, $f_{OUT} = 697Hz$	C_2 Only		480		mV
			C_1 to C_2		480		mV
			No filtering		490		mV
		$R_L = 1k\Omega$, $f_{OUT} = 1633Hz$	C_1		490		mV
			C_1 to C_2		580		mV
			No filtering		655		mV
Skew Between High and Low Band Output Voltages		$R_L = 1k\Omega$, C_1, C_2 disconnected			2.5	3.0	dB
Output Impedance	Z_O	$R_L = 1k\Omega$	Operating		90	200	Ω
			Quiescent		25		KΩ
Total Output Harmonic Distortion	THD1	Either Hi or Low Bands			20	25	%
		No Low Pass Filtering					%
Total Output Harmonic Distortion	THD2	$R_L = 1k\Omega$, $C_1 = .002\mu F$	$f_{OUT} = 697Hz$		2.3	10	%
		$C_2 = 0.02\mu F$	$f_{OUT} = 1633Hz$		1.0	10	%
Maximum Output Voltage Level	V_{OH}	$R_L = 1k\Omega$				4.6	V
Minimum Output Voltage Level	V_{OL}	$R_L = 1k\Omega$		0.5			V
Keyboard Input Pullup Resistors	R_{IN}	Terminals 3,4,5,6,11,12,13,14		35	100	150	KΩ
Keyboard Input Capacitance	C_{IN}	Terminals 3,4,5,6,11,12,13,14				5	pF
Guaranteed Oscillator Frequency Range (Note 4)	f_{OSC}	$3 \le (V^+ - V^-) \le 6V$		2.0		4.5	MHz
Guaranteed Oscillator Frequency Range		$4V \le (V^+ - V^-) \le 6V$		2.0		7	MHz
System Startup Time on Application of Power	t_{on}	ICM7206, ICM7206A			10		ms
System Startup Time on Application of Power and Key Depressed Simultaneously		ICM7206B, ICM7206C, ICM7206D				7	ms
DISABLE Output Saturation Resistance (ON STATE)	R_D	See Logic Table for Input Conditions Current = 4mA			330	700	Ω
DISABLE Output Leakage (OFF STATE)	I_{OLK}	See Logic Table for Input Conditions				10	μA
Oscillator Load Capacitance	C_{OSC}	Measured between terminals 9 & 10, no supply voltage applied to circuit $-40°C \le T_A \le 85°C$			7		pF
Guaranteed Output Frequency Tolerance	f_O	Any output frequency Crystal tolerance ±60ppm Crystal load capacitance CL = 30pF				±0.75	%
Oscillator Startup Time ICM7206B, C, D	t_{start}	$V^+ = 3V$ (Note 5)				7	ms

NOTE 3: Operation above 6 volts must employ supply current limiting. Refer to 'ABSOLUTE MAXIMUM RATINGS' and the Application Notes for further information.

NOTE 4: The ICM7206 family uses dynamic high frequency circuitry in the initial 2^3 divider resulting in low power dissipation and excellent performance over a restricted frequency range. Thus, for reliable operation with a 6 volt supply an oscillator frequency of not less than 2MHz must be used.

NOTE 5: After row input is enabled.

TRUTH TABLE

LINE	ROWS (1) ACTIVATED	COLS (2) ACTIVATED	OUTPUT (TERMINAL #15)	DISABLE (TERMINAL #7)	COMMENTS
1	0	0	Off	Off	Quiescent State
2	1	1	$f_{row} + f_{col}$	On	Dual Tone
3	1	2 or 3 (incl. col #4)	f_{row}	On	Single Tone
4	2 or 3	1	f_{col}	On	Single Tone
5	2 or 3	2 or 3 (excl. col #3)	D.C. Level	On	No Tone
6	1	4 or 3 (must excl. col #4)	f_{row}, 50% Duty Cycle	f_{row}, 50% Duty Cycle	f_{row} Test
7	4	1	f_{col}, 50% Duty Cycle	f_{col}, 50% Duty Cycle	f_{col} Test
8	0	1 or 2 or 3 or 4	Off	Off	n/a*
9	1	0	902Hz + f_{row}	On	n/a*
10	2 or 3	0	902Hz	On	n/a*
11	4	0	902Hz, 50% Duty Cycle	902Hz, 50% Duty Cycle	n/a*
12	2 or 3 or 4	4	D.C. Level	Indeterminate	Multiple Key Lockout
13	4	2 or 3 or 4	D.C. Level	Indeterminate	Multiple Key Lockout

*n/a — not applicable to telephone calling.

Note 1: Rows are activated for the ICM7206/C by connecting to a negative supply voltage with respect to V^+ (terminal 16) at least 33% of the value of the supply voltage (V^+–V^-). For the ICM7206A rows (and columns) are activated by connecting to a positive supply voltage with respect to V^- (terminal 8) at least 33% of the value of the supply voltage (V^+–V^-). The rows and columns of the ICM7206B are activated by connecting to a negative supply voltage.

Note 2: Columns (ICM7206) are activated by being connected to a positive supply voltage with respect to V^- (terminal 8) at least 33% of the value of the supply voltage (V^+–V^-).

COMMENTS

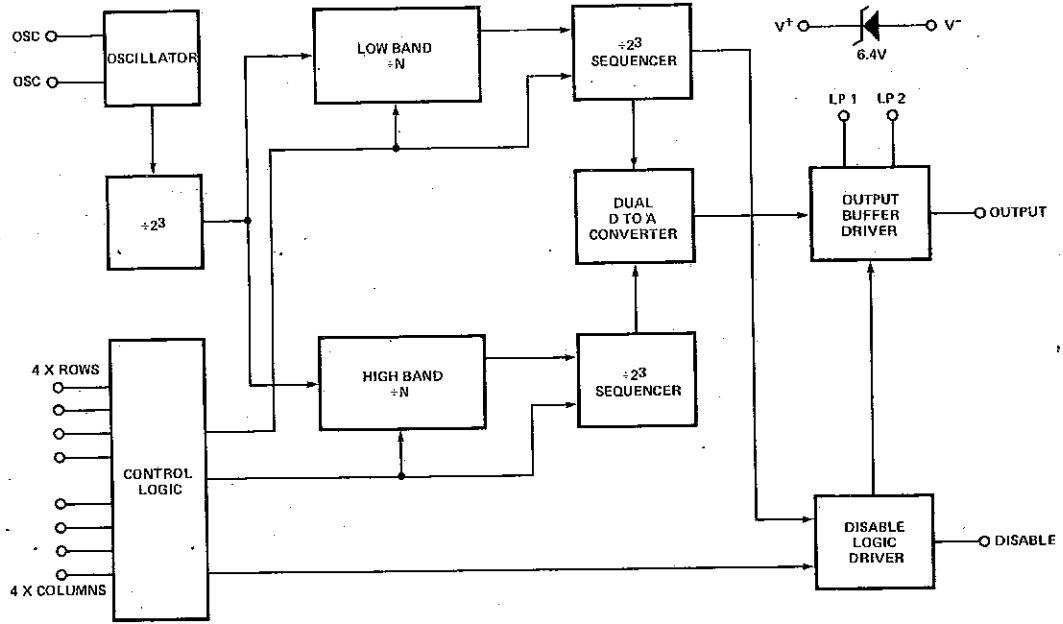
All combinations of row and column activations are given in the truth table. Lines 1 thru 7 and 12, 13 represent conditions obtainable with a matrix keyboard. Lines 8 thru 11 are given only for completeness and are not pertinent to telephone dialing.

Lines 6 and 7 show conditions for generating 50% duty cycle full amplitude signals useful for rapid testing of the row and column frequencies on automatic test equipment. In all other cases, output frequencies on terminal 15 are single or dual 4 level synthesized sine waves.

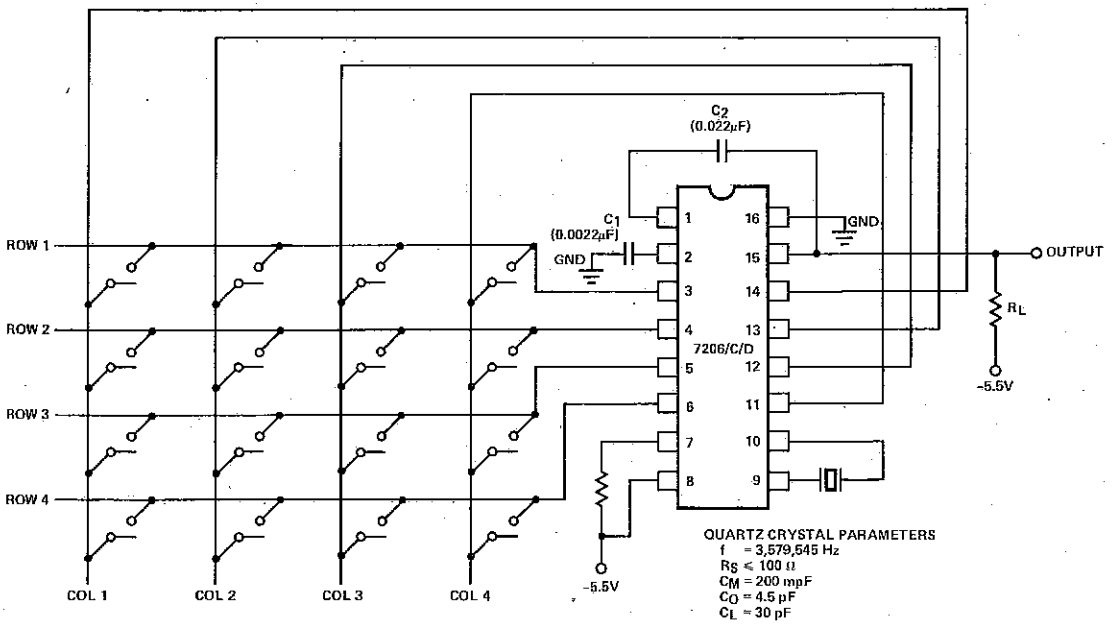
A 'DC LEVEL' on terminal 15 may be any voltage level between approximately 1.2 and 4.3 volts with respect to V^- (terminal 8) for a 5.5 volt supply voltage.

The impedance of the OUTPUT (terminal 15) is approximately 20K ohms in the OFF state. The 'DISABLE OUT-OUT' ON and OFF conditions are defined in the TYPICAL OPERATING CHARACTERISTICS.

SCHEMATIC DIAGRAM

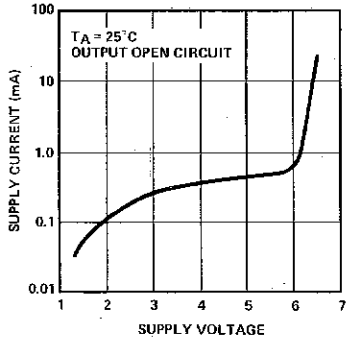


TEST CIRCUIT (single contact keyboard devices shown)

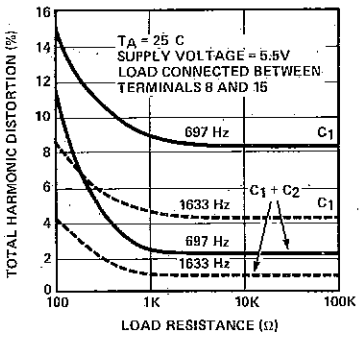


TYPICAL OPERATING CHARACTERISTICS

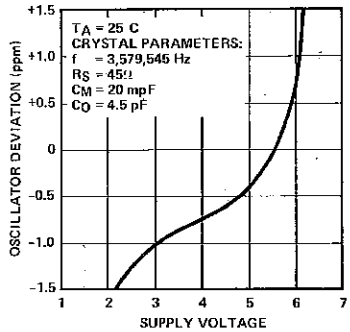
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



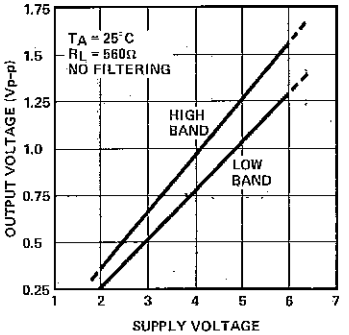
TOTAL HARMONIC DISTORTION AS A FUNCTION OF LOAD RESISTANCE

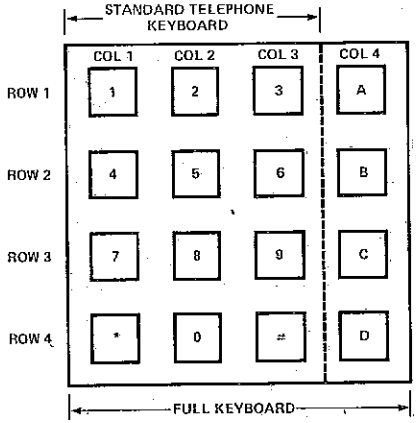


OSCILLATOR FREQUENCY DEVIATION AS A FUNCTION OF SUPPLY VOLTAGE



PEAK TO PEAK OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE





KEY	LOW BAND FREQ. Hz	HI BAND FREQ. Hz
1	697	1209
2	697	1336
3	697	1477
4	770	1209
5	770	1336
6	770	1477
7	852	1209
8	852	1336
9	852	1477
*	941	1209
0	941	1336
#	941	1477
A	697	1633
B	770	1633
C	852	1633
D	941	1633

FIGURE 1: Keyboard Frequencies

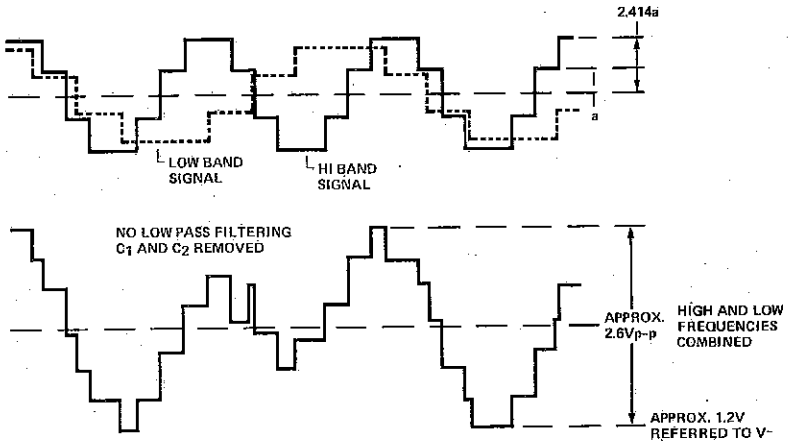


FIGURE 2

Figure 2 shows individual currents of a low band and high band frequency pair into the summing node A (see Figure 3) and the resultant voltage waveform.

DESIRED FREQUENCY Hz	ACTUAL FREQUENCY Hz	FREQUENCY DEVIATION %	DIVIDE BY N RATIO
697	699.13	+0.30	80
770	766.17	−0.50	73
852	847.43	−0.54	66
941	947.97	+0.74	59
1209	1215.88	+0.57	46
1336	1331.68	−0.32	42
1477	1471.85	−0.35	38
1633	1645.01	+0.74	34

APPLICATION NOTES

1. Device Description

The ICM7206 family is manufactured with a standard metal gate C-MOS technology having proven reliability and excellent reproducability resulting in extremely high yields. The techniques used in the design have been developed over many years and are characterized by wide operating supply voltage ranges and low power dissipation.

To minimize chip size, all diffusions used to define source-drain regions and field regions are butted up together. This results in approximately 6.3 volt zener breakdown between the supply terminals, and between all components on chip. As a consequence, the usual C-MOS static charge problems and handling problems are not experienced with the ICM7206.

The oscillator consists of a medium size C-MOS inverter having on chip a feedback resistor and two capacitors of 14pF each, one at the oscillator input and the other at the oscillator output. The oscillator is followed by a dynamic ÷23 circuit which divides the oscillator frequency to 447,443Hz. This is applied to two programmable dividers each capable of division ratios of any integer between 1 and 128, and each counter is controlled by a ROM. The outputs from the programmable counters drive sequencers (divide by 8) which generate the eight time slots necessary to synthesize the 4-level sine waves.

The control logic block recognizes signals on the row and column inputs that are only a small fraction of the supply voltage, thereby permitting the use of a simple matrix single contact per key keyboard, rather than the more usual two contacts per key type having a common line. The row and column pullup resistors are equal in value and connected to the opposite supply terminals (ICM7206/C only; for the ICM7206A all pullup resistors are connected to the V^- terminal and for the ICM7206B they are tied to the V^+. Therefore, connecting a row input to a column input generates a voltage on those inputs which is one half of the supply voltage.

The ICM7206 family employs a unique but extremely simple digital to analog (D to A) converter. This D to A converter produces a 4 level synthesized sine wave having an intrinsic total harmonic distortion level of approximately 20%. Figure 3 shows a single channel D to A converter. The current sources Q_2 and Q_3 are proportioned in the ratio of 1:1.414. During time slots 1 and 8 both S_1 and S_2 are off, during time slots 2 and 7 only S_1 is on, during time slots 3 and 6 only S_2 is on, and during time slots 4 and 5 both S_1 and S_2 are on. The resultant currents are summed at node A, buffered by Q_4 and further buffered by R_3, R_4 and Q_5. Switch S_3 allows the output to go into a high impedance mode under quiescent conditions.

Node A is the common summing point for both the high and low band frequencies although this is not shown in Figure 3.

The synthesized sine wave has negligible even harmonic distortion and very low values of third and fifth harmonic distortion thereby minimizing the filtering problems necessary to reduce the total harmonic distortion to well below the 10% level required for touch tone telephone encoding. Figure 4 shows the low pass filter characteristic of the output buffer for $C_1 = 0.0022\mu F$ and $C_2 = 0.022\mu F$. A small peak of 0.4dB occurs at 1100Hz with sharp attention (12dB per octave) above 2500Hz. This type of active filter produces a sharper and more desirable knee characteristic than would two simple cascaded RC networks.

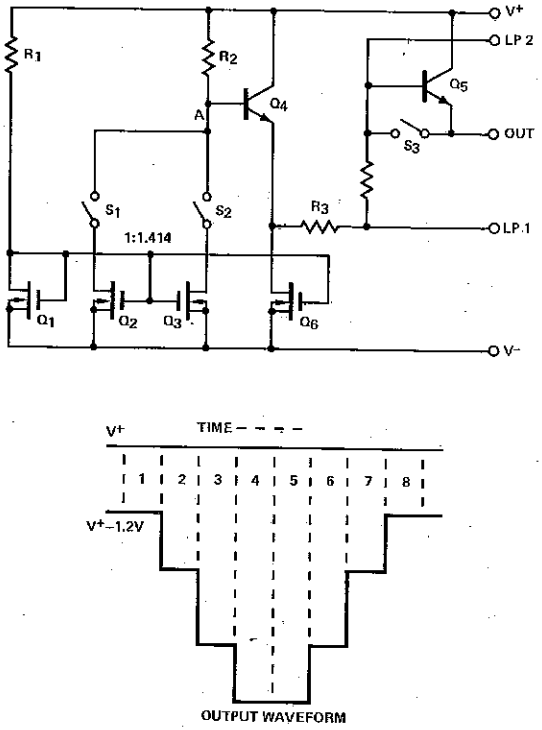


FIGURE 3: D to A Converter and Output Buffer

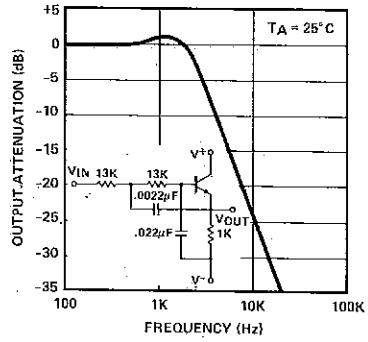


FIGURE 4: Frequency Attentuation Characteristics of the Output Buffer

2. Latchup Considerations

Most junction isolated C-MOS integrated circuits, especially those of moderate or high complexity, exhibit latchup phenomena whereby they can be triggered into an uncontrollable low impedance mode between the supply terminals. This can be due to gross forward biasing of inputs or outputs (with respect to the supply terminals), high voltage supply transients, or more rarely by exceptional fast rate of rise of supply voltages.

The ICM7206 family is no exception, and precautions must be taken to limit the supply current to those values shown in the ABSOLUTE MAXIMUM RATINGS. For an example, do not use a 6 volt very low impedance supply source in an **electrically extremely noisy** environment unless a 500 ohm current limiting resistor is included in series with the V^- terminal. For normal telephone encoding applications no problems are envisioned, even with low impedance transients of 100 volts or more, if circuitry similar to that shown in the next section is used.

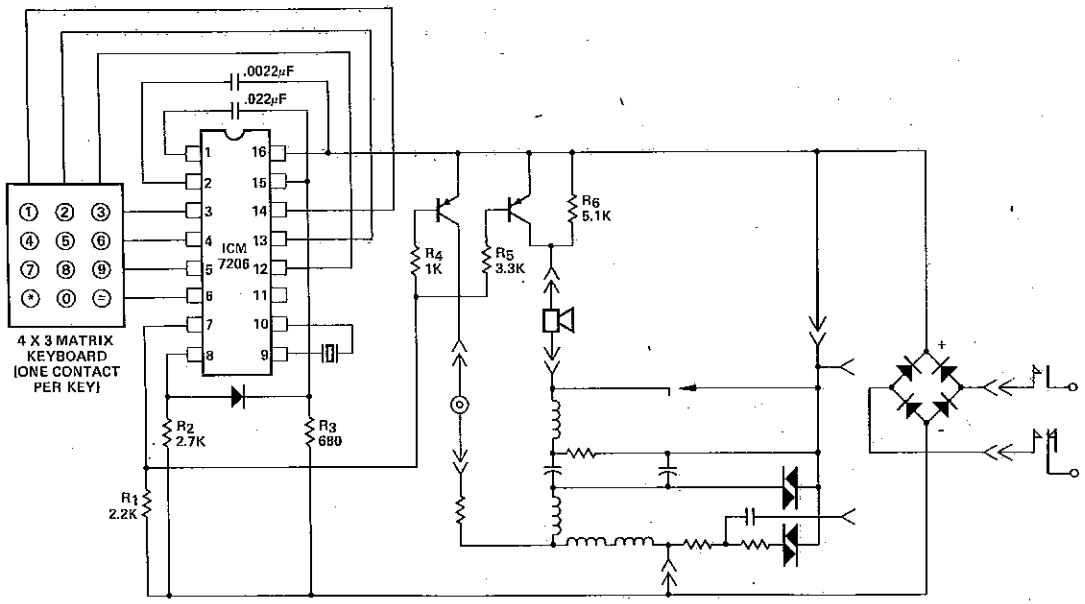
3. Typical Application (Telephone Handset)

A typical encoder for telephone handsets is shown in Figure 5. This encoder uses a single contact per key keyboard and provides all other switching functions electronically. The diode connected between terminals 8 and 15 prevents the output going more than 1 volt negative with respect to the negative supply V^- and the circuit operates over the supply voltage range from 3.5 volts to 15 volts on the device side of the bridge rectifier. Transients as high as 100 volts will not cause system failure, although the encoder will not operate correctly under these conditions. Correct operation will resume immediately after the transient is removed.

The output voltage of the synthesized sine wave is almost directly proportional to the supply voltage (V^+–V^-) and will increase with increase of supply voltage until zener breakdown occurs (approximately 6.3 volts between terminals 8 and 16) after which the output voltage remains constant.

4. Portable Tone Generator

The ICM7206A/B require a two contact key keyboard with the common line connected to the positive supply (neg for ICM7206B) (terminal 16). A simple diode matrix may be used with this keyboard to provide power to the system whenever a key is depressed, thus avoiding the need for an on/off switch. In Figure 6 the tone generator is shown using a 9 volt battery. However, if instead, a 6 volt battery is used, the diode D_4 is not required. It is recommended that a 470 ohm resistor still be included in series with a negative (positive) supply to prevent accidental triggering of latchup.



NOTE: If dual contact keyboard is used, common should be left floating.

FIGURE 5: Telephone Handset Touch Tone Encoder

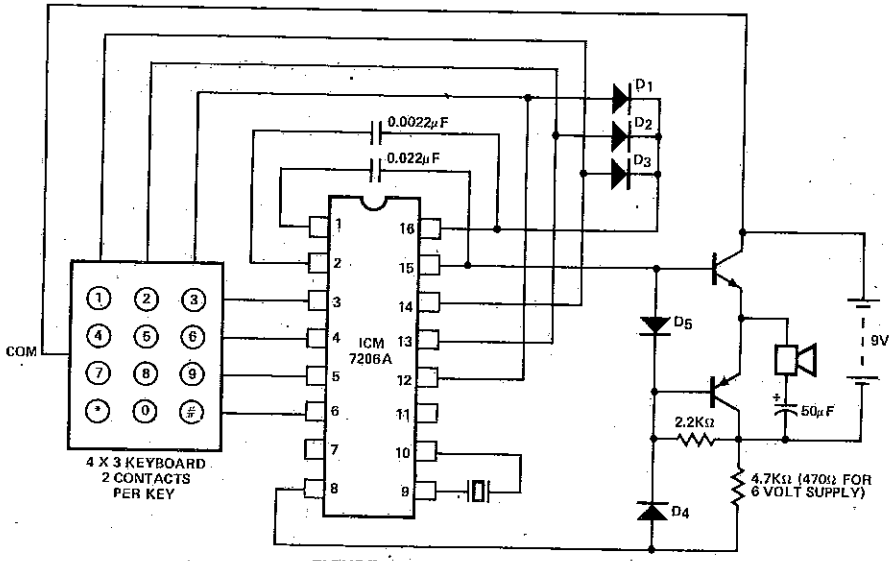


FIGURE 6: Portable Tone Generator

OPTIONS

(For additional information consult the factory)

Options can be achieved using metal mask additions to provide the following.

1) The sequence or position of either the row or column terminals can be interchanged i.e., row 1 terminal 3 could become terminal 11, etc.

2) Any frequency oscillator from approximately 0.5MHz to 7MHz can be chosen. Note that the accuracy of the output frequencies will depend on the exact oscillator frequency. For instance, a 1 MHz crystal could be used with worst case output frequency error of 0.8%. Or, if high accuracy is required, ±0.25%, oscillator frequencies of 5,117,376Hz or 2,558,688Hz could be selected. ROM's are used to program the dividers.

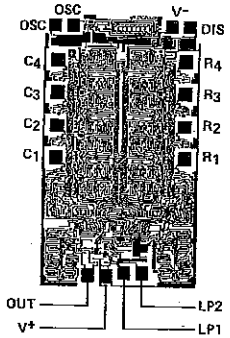
3) The 'DISABLE' output may be changed to an inverter or an uncommitted drain n-channel transistor.

4) The oscillator may be disabled until a key is depressed.

CHIP TOPOGRAPHY

Chip Dimensions
0.60" (1.524mm)x0.101"
(2.565mm)

Chip may be die attached using conventional eutectic or epoxy procedures. Wire bonding may be either aluminum ultrasonic or gold compression.



ICM7209
CMOS Clock Generator

FEATURES

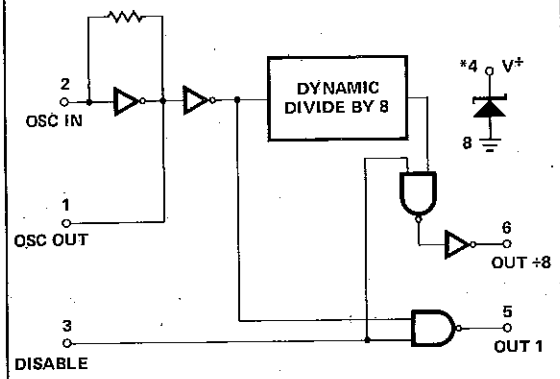
- High frequency operation — 10MHz guaranteed
- Easy to use oscillator — requires only a quartz crystal and two capacitors
- Bipolar, MOS and CMOS compatibility
- High output drive capability — 5 x TTL fanout with 10ns rise and fall times
- Low power — 50mW at 10MHz
- Choice of two output frequencies — osc., and osc. ÷8 frequencies
- Disable control for both outputs
- Wide industrial temperature range — −20°C to +85°C
- All inputs fully protected — circuits may be handled without any special precautions

GENERAL DESCRIPTION

The Intersil ICM7209 is a versatile CMOS clock generator capable of driving a number of 5 volt systems with a variety of input requirements. When used to drive up to 5 TTL gates, the typical rise and fall times are 10ns.

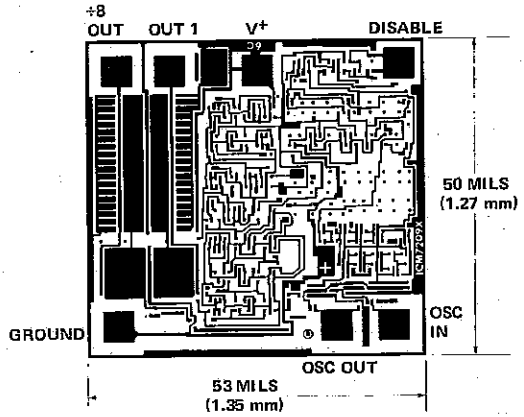
The ICM7209 consists of an oscillator, a buffered output equal to the oscillator frequency and a second buffered output having an output frequency one-eighth that of the oscillator. The guaranteed maximum oscillator frequency is 10MHz. Connecting the DISABLE terminal to the negative supply forces the ÷8 output into the '0' state and the output 1 into the '1' state.

SCHEMATIC DIAGRAM

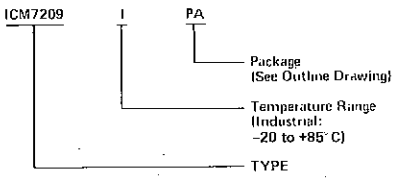


*ZENER VOLTAGE IS TYPICALLY 6.3 VOLTS

CHIP TOPOGRAPHY



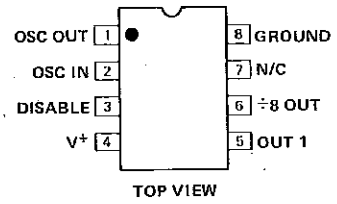
ORDERING INFORMATION



Order Devices by Following Part Number ICM7209 I PA

Order Dice by Following Part Number ICM7209/D

PIN CONFIGURATION (OUTLINE DRAWING PA)



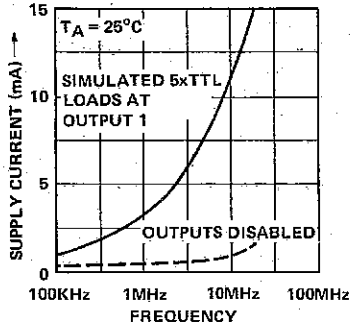
TOP VIEW

Pin 1 is designated by either a dot or a notch.

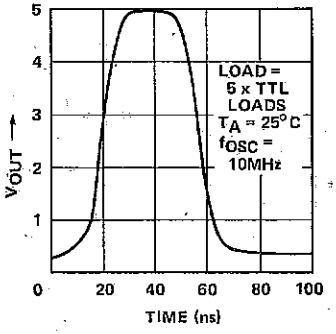
7

TYPICAL OPERATING CHARACTERISTICS

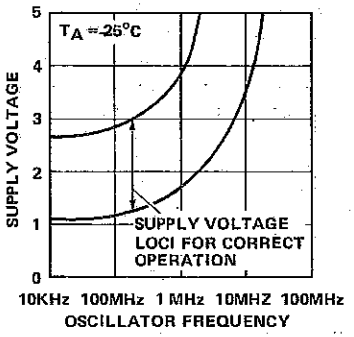
SUPPLY CURRENT AS A FUNCTION OF OSCILLATOR FREQUENCY



TYPICAL OUT 1 RISE AND FALL TIMES



SUPPLY VOLTAGE RANGE FOR CORRECT OPERATION OF ÷8 COUNTER AS A FUNCTION OF OSCILLATOR FREQUENCY



Rise and fall times of OUT ÷8 are similar to those of OUT 1.

7

APPLICATION NOTES

OSCILLATOR CONSIDERATIONS

The oscillator consists of a C-MOS inverter with a non-linear resistor connected between the oscillator input and output to provide D.C. biasing. Using commercially obtainable quartz crystals the oscillator will operate from low frequencies (10KHz) to 10MHz.

The oscillator circuit consumes about 500μA of current using a 10MHz crystal with a 5 volt supply, and is designed to operate with a high impedance tank circuit. It is therefore necessary that the quartz crystal be specified with a load capacitance (C_L) of 10pF instead of the standard 30pF. To maximize the stability of the oscillator as a function of supply voltage and temperature, the motional capacitance of the crystal should be low (5mpF or less). Using a fixed input capacitor of 18pF and a variable capacitor of nominal value of 18pF on the output will result in oscillator stabilities of typically 1ppm per volt change in supply voltage.

THE ÷8 OUTPUT

A dynamic divider is used to divide the oscillator frequency by 8. Dynamic dividers use small nodal capacitances to store

dividers). The dynamic divider has advantages in high speed operation and low power but suffers from limited low frequency operation. This results in a window of operation for any oscillator frequency (see graph under TYPICAL OPERATING CHARACTERISTICS).

OUTPUT DRIVERS

The output drivers consist of C-MOS inverters having active pullups and pulldowns. Thus the outputs can be used to directly drive TTL gates, other C-MOS gates operating with a 5 volt supply, or TTL compatible MOS gates.

The guaranteed fanout is 5 TTL loads although typical fanout capability is at least 10 TTL loads with slightly increased output rise and fall times.

COMMENTS ON THE DEVICE POWER CONSUMPTION

At low frequencies the principal component of the power consumption is the oscillator. At high oscillator frequencies the major portion of the power is consumed by the output drivers, thus by disabling the outputs (activating the DISABLE INPUT) the device power consumption can be

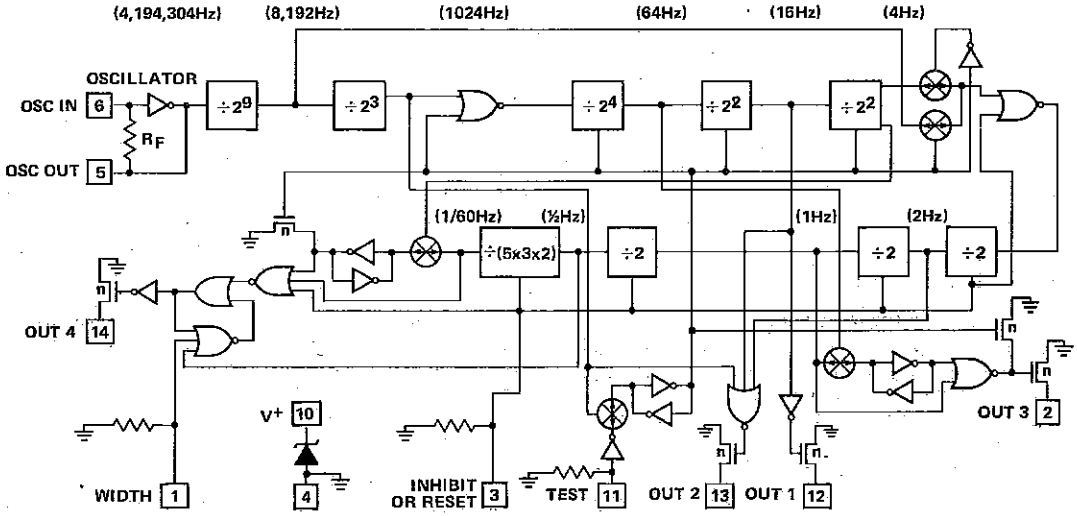
ICM7213
One Second/One Minute Precision Clock and Reference Generator

FEATURES
- Guaranteed 2 volts operation
- Very low current consumption: Typ. 100μA @ 3V
- All outputs TTL compatible
- On chip oscillator feedback resistor
- Oscillator requires only 3 external components: fixed capacitor, trim capacitor, and a quartz crystal
- Output inhibit function
- 4 simultaneous outputs: one pulse/sec, one pulse/min, 16Hz and composite 1024 + 16 + 2Hz outputs
- Test speed-up provides other frequency outputs
- Input static protection — no special handling required

GENERAL DESCRIPTION
The ICM7213 is a fully integrated micropower oscillator and frequency divider with four buffered outputs suitable for interfacing with most logic families. The power supply may be either a two battery stack (Ni-cad, alkaline, etc.) or a regular power supply greater than 2 volts. Depending upon the state of the WIDTH, INHIBIT, and TEST inputs, using a 4.194304 MHz crystal will produce a variety of output frequencies including 2048 Hz, 1024 Hz, 34.133 Hz, 16 Hz, 1 Hz, and 1/60 Hz (plus composites).

The ICM7213 utilizes a very high speed low power metal gate C-MOS technology which uses 6.4 volt zeners between the drains and sources of each transistor and also across the supply terminals. Consequently, the ICM7213 is limited to a 6 volt maximum supply voltage, although a simple dropping network can be used to extend the supply voltage range well above 6 volts (see Figure 2).

BLOCK DIAGRAM



ORDERING INFORMATION

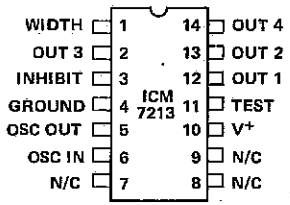
ICM7213 I PD

- PD — Package: PD = 14 Pin Plastic
- I — Temperature Range: -20°C to +85°C
- ICM7213 — Type

Order Devices by Following Part Number
ICM7213IPD

Order Dice by Following Part Number
ICM7213D

PIN CONFIGURATION (OUTLINE DRAWING PD)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6.0V
Output Current (Any output) 20mA
All Input and Oscillator Voltages (Note 1) ..... Equal to but not greater than the supply voltage
All Output Voltages (Note 1) ..... $0 \leq V_O \leq +6$
Operating Temperature Range ..... -20°C to +85°C
Storage Temperature Range ..... -40°C to +125°C
Power Dissipation (Note 2) 200mW
Lead Temperature (Soldering 10 sec.) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: The ICM7213 like most C-MOS devices, may enter a destructive latchup mode if an input or output voltage is applied in excess of those defined and there is no supply current limiting.

NOTE 2: Derate linearly power rating of 200mW at 25°C to 50mW at 70°C.

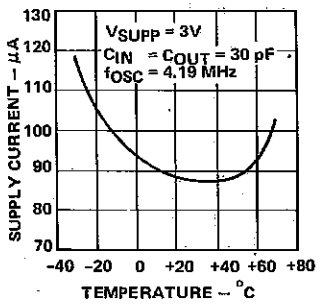
OPERATING CHARACTERISTICS

TEST CONDITIONS: V+ = 3.0V, f_{osc} = 4.194304 MHz, Test Circuit, T_A = 25°C unless otherwise specified

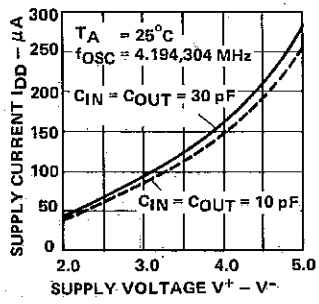
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I^+			100	140	µA
Guaranteed Operating Supply Voltage Range	V_{OP}	-20°C < T_A < 85°C	2		4	V
Output Leakage Current	I_{OLK}	Any output, V_{OUT} = 6 Volts			10	µA
Output Sat. Resistance	R_{OUT}	Any output, I_{OLK} = 2.5mA		120	200	Ω
Inhibit Input Current.	I_I	Inhibit terminal connected to V^+		10	40	µA
Test Point Input Current	I_{TP}	Test point terminal connected to V^+		10	40	
Width Input Current	I_W	Width terminal connected to V^+		10	40	
Oscillator g_m	g_m	V^+ = 2V	100			umho
Oscillator Frequency Range (Note 3)	f_{osc}		1		10	MHz
Oscillator Stability	f_{STAB}	2V < V^+ < 4V		1.0		ppm
Oscillator Start Time	t_s	V^+ = 3.0 volts		0.1		sec
		V^+ = 2.0 volts		0.2		

NOTE 3: The ICM7213 uses dynamic dividers for high frequency division. As with any dynamic system, information is stored on very small nodal capacitances instead of latches (static system), therefore there is a lower frequency of operation. Dynamic dividers are used to improve the high frequency performance while at the same time significantly decreasing power consumption. At low supply voltages, operation at less than 1MHz is possible. See application notes.

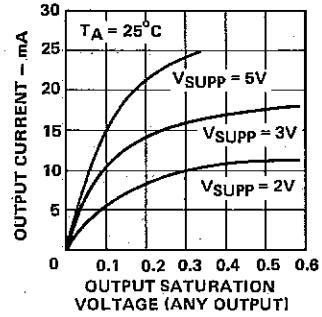
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



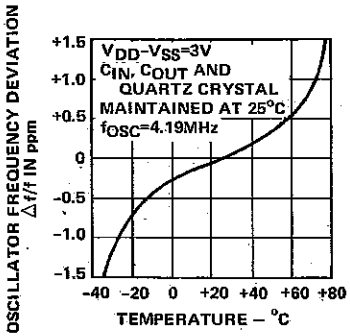
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



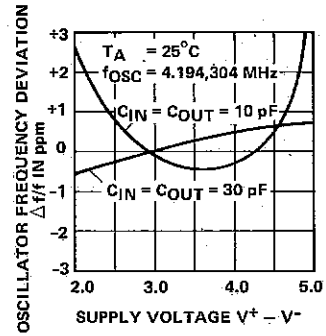
OUTPUT CURRENT AS A FUNCTION OF OUTPUT SATURATION VOLTAGE



OSCILLATOR STABILITY AS A FUNCTION OF DEVICE TEMPERATURE

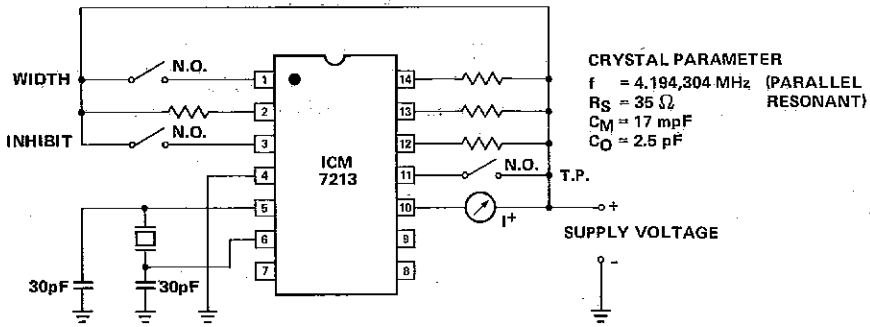


OSCILLATOR STABILITY AS A FUNCTION OF SUPPLY VOLTAGE



7

TEST CIRCUIT



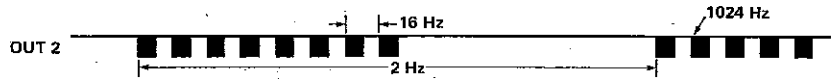
OUTPUT DEFINITIONS

TABLE I.

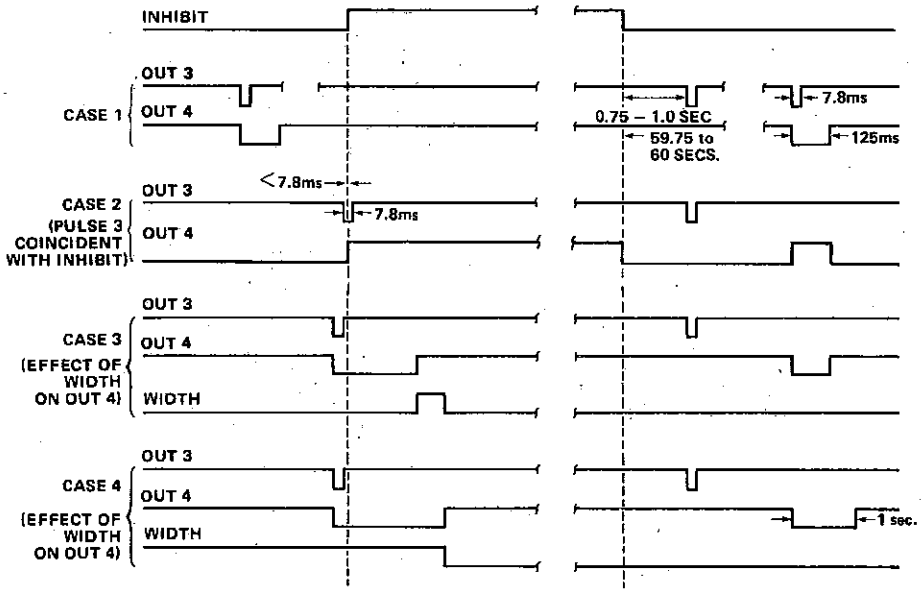
INPUT STATES*			PIN 12	PIN 13	PIN 2	PIN 14
TEST	INHIBIT	WIDTH	OUT 1	OUT 2	OUT 3	OUT 4
L	L	L	16Hz ÷2^{18}	$\overline{1024 + 16 + 2}$Hz (÷2^{12}÷2^{18}÷2^{21}) composite	1Hz, 7.8mS ÷2^{22}	1/60Hz, 1 Sec. ÷ (2^{24} x 3 x 5)
L	L	H	16Hz ÷2^{18}	$\overline{1024 + 16 + 2}$Hz (÷2^{12}÷2^{18}÷2^{21}) composite	1Hz, 7.8mS ÷ 2^{22}	1/60Hz, 125ms
L	H	L	16Hz ÷2^{18}	$\overline{1024 + 16}$Hz (÷2^{12}÷2^{18}) composite	OFF	OFF
L	H	H	16Hz ÷2^{18}	$\overline{1024 + 16}$Hz (÷2^{12}÷2^{18}) composite	OFF	SEE WAVEFORMS
H	L	L	ON	$\overline{4096 + 1024}$Hz (÷2^{10}÷2^{12}) composite	2048Hz ÷2^{11}	34.133Hz, 50% D.C. ÷(2^{13} x 5 x 3)
H	L	H	ON	$\overline{4096 + 1024}$Hz (÷2^{10}÷2^{12}) composite	2048Hz ÷2^{11}	34.133Hz, 50% D.C. ÷(2^{13} x 5 x 3)
H	H	L	ON	1024Hz ÷2^{12}	ON	OFF
H	H	H	ON	1024Hz ÷2^{12}	ON	OFF

NOTE: When TEST and RESET are connected to ground, or left open, all outputs except for OUT 3 and OUT 4 have a 50% duty cycle.

OUTPUT WAVEFORMS



EFFECT OF INHIBIT INPUT TEST connected to ground or left open.



All time scales are arbitrary, and in the case of OUT 3 only the shown. Where time intervals are relevant they are clearly

APPLICATIONS

1. Supply Voltage Considerations

The ICM7213 may be used to provide various precision outputs with frequencies from 2048Hz to 1/60Hz using a 4,194,304Hz quartz oscillator, and other output frequencies may be obtained using other quartz crystal frequencies. Since the ICM7213 uses dynamic high frequency dividers for the initial frequency division there are limitations on the supply voltage range depending on the oscillator frequency. If, for example, a low frequency quartz crystal is selected, the supply voltage should be selected in the center of the operating window, or approximately 1.7 volts.

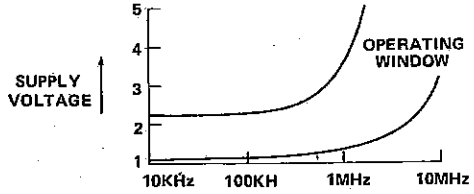
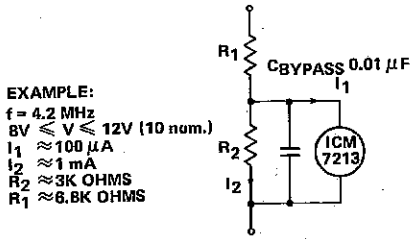


FIGURE 1: Window of Correct Operation

The supply voltage to the ICM7213 may be derived from a high voltage supply by using a simple resistor divider (if power is of no concern), by using a series resistor for minimum current consumption, or by means of a regulator.



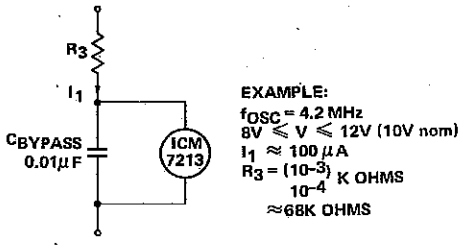


FIGURE 2: Biasing Schemes with High Voltage Supplies

2. Logic Family Compatability

Pull up resistors will generally be required to interface with other logic families. These resistors must be connected between the various outputs and the positive power supply.

3. Oscillator Considerations

The oscillator consists of a C-MOS inverter and a feedback resistor whose value is dependent on the voltage at the oscillator input and output terminals and the supply voltage. Oscillator stabilities of approximately 0.1ppm per 0.1 volt variation are achievable with a nominal supply voltage of 5 volts and a single voltage dropping resistor. The crystal specifications are shown in the TEST CIRCUIT.

It is recommended that the crystal load capacitance (CL) be no greater than 22pF for a crystal having a series resistance equal to or less than 75 ohms, otherwise the output amplitude of the oscillator may be too low to drive the divider reliably.

If a very high quality oscillator is desired, it is recommended that a quartz crystal be used having a tight tuning tolerance ±10ppm, a low series resistance (less than 25 ohms), a low motional capacitance of 5mpF and a load capacitance of 20pF. The fixed capacitor C_{IN} should be 30pF and the oscillator tuning capacitor should range between approximately 16 and 60pF.

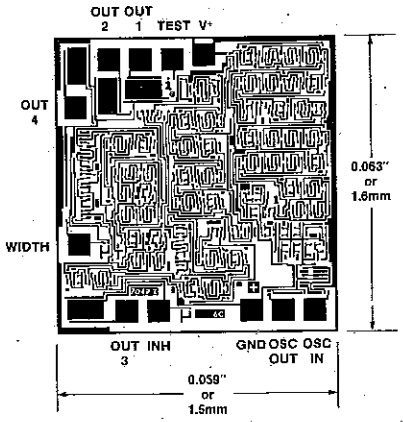
Use of a high quality crystal will result in typical stabilities of 0.05ppm per 0.1 volt change of supply voltage.

4. Control Inputs

The TEST input inhibits the 2^{18} output and applies the 2^9 output to the 2^{21} divider, thereby permitting a speedup of the testing of the ÷60 section by a factor of 2048 times. This also results in alternative output frequencies (see table).

The WIDTH input may be used to change the pulse width of OUT 4 from 125ms to 1 sec, or to change the state of OUT 4 from ON to OFF during INHIBIT.

CHIP TOPOGRAPHY



ICM7215
6-Digit 4-Function LED Stopwatch Circuit

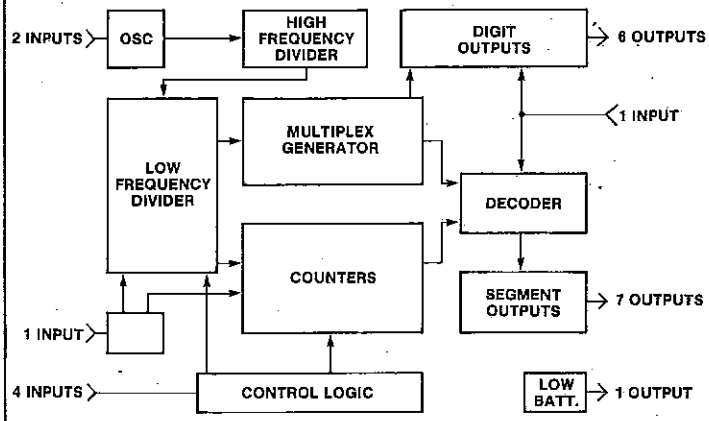
FEATURES

- **Four functions: start/stop/reset, split, taylor, time out**
- **Six digit display: ranges up to 59 minutes 59.99 seconds**
- **High LED drive current: 13mA peak per segment at 16.7% duty cycle with 4.0 volt supply**
- **Requires only three low cost SPST switches without loss of accuracy: start/stop, reset, display unlock**
- **Chip enable pin turns off both segment and digit outputs; can be used for multiple circuits driving one display**
- **Low battery indicator**
- **Digit blanking on seconds and minutes**
- **Wide operating range: 2.0 to 5.0 volts**
- **1KHz multiplex rate prevents flickering display**
- **Can be used easily in four different single function stopwatches or two two-function stopwatches: start/stop/reset with time-out, split with taylor. The component count for a three- or four-function stopwatch will be slightly greater.**
- **Retrofit to ICM7205 for split and/or taylor applications**

GENERAL DESCRIPTION

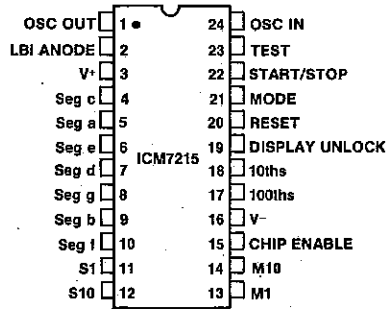
The ICM7215 is a fully integrated six digit LED stopwatch circuit fabricated with Intersil's low threshold metal gate CMOS process. The circuit interfaces directly with a six digit/seven segment common cathode LED display. The low battery indicator can be connected to the decimal point anode or to a separate LED. The only components required for a complete stopwatch are the display, three SPST switches, a 3.2768MHz crystal, a trimming capacitor, three AA batteries and an on-off switch. For a two function stopwatch, or to add a display off feature, one additional slide switch is required. The circuit divides the oscillator frequency by 2^{15} to obtain 100Hz, which is fed to the fractional seconds, seconds and minutes counters, while an intermediate frequency is used to obtain the 1/6 duty cycle 1.07KHz multiplex waveforms. The blanking logic provides leading zero blanking for seconds and minutes independently of the clock. The ICM7215 is packaged in a 24-lead plastic DIP.

BLOCK DIAGRAM



PIN CONFIGURATION

(OUTLINE DRAWING PG)



ORDERING INFORMATION

Order devices by following part number ICM7215 I PG
Order dice by following part number ICM7215/D

7

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... 5.5 V
Power Dissipation (Note 1) ..... 0.75 W
Operating Temperature ..... −20°C to +70°C
Storage Temperature ..... −55°C to +125°C
Input and Output Voltage ..... equal to but never exceeding the supply voltage

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS:

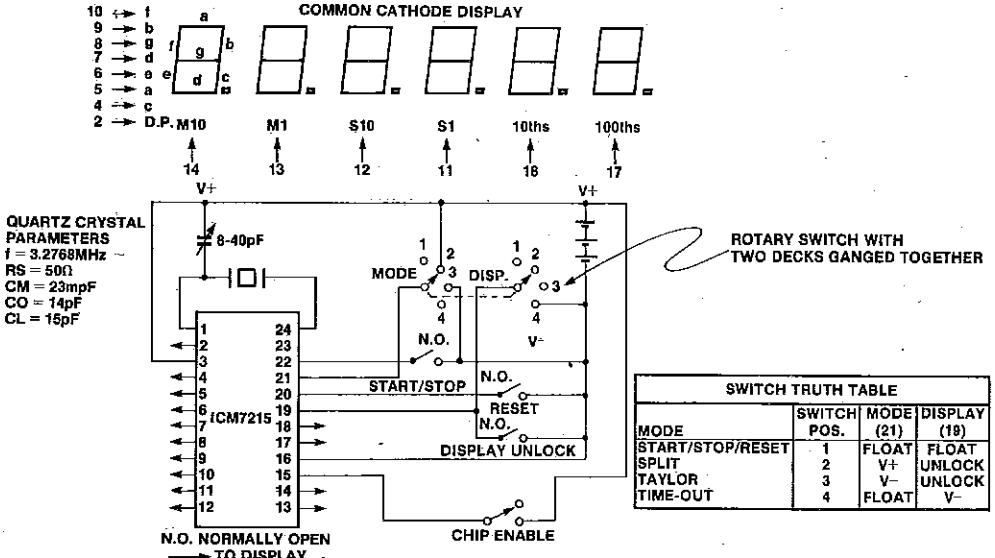
TEST CONDITIONS: $T_A = +25°C$, stopwatch circuit, $V^+ = 4.0V$ unless otherwise specified.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V^+	$-20°C \le T_A \le +70°C$	2.0		5.0	V
Supply Current	I^+	Display off		0.6	1.5	mA
Segment Current	I_{SEG}	5 segments lit				mA
Peak		1.8 Volts across display	9.0	13.2		
Average				2.2		
Switch Actuation Current	I_{SW}	All inputs except chip enable		20	50	µA
Switch Actuation Current		Chip enable		50	200	
Digit Leakage Current	I_{DLK}	$V_{DIG} = 2.0V$			50	
Segment Leakage Current	I_{SLK}	$V_{SEG} = 2.0V$			100	
Low Battery Indicator Trigger Voltage	V_{LBI}		2.2		2.8	V
LBI Output Current	I_{LBI}	$V^+ = 2.0V$, $V_{LBI} = 1.6V$		2.0		mA
Oscillator Stability	f_{STAB}	$V^+ = 2.0V$ to $V^+ = 5.0V$		6		PPM
Oscillator Transconductance	g_m	$V^+ = 2.0V$	120			µmho
Oscillator Input Capacitance	C_{OSCI}		24	30	36	pF

NOTE 1: The output devices on the ICM7215 have very low impedance characteristics, especially the digit cathode drivers. If these devices are shorted to a low impedance power supply, the current could be as high as 300mA. This will not damage the device momentarily, but if the short circuit condition is not removed immediately probable device failure will occur.

7

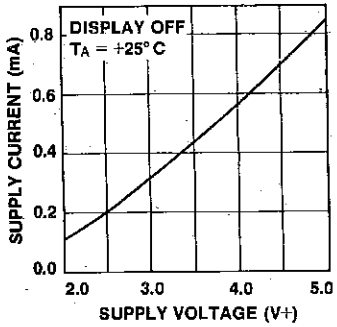
STOPWATCH CIRCUIT



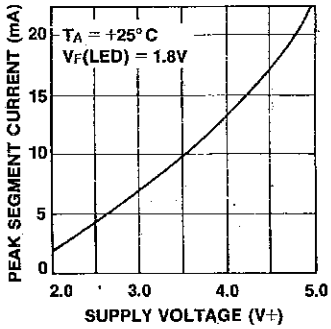
SWITCH TRUTH TABLE			
MODE	SWITCH POS.	MODE (21)	DISPLAY (19)
START/STOP/RESET	1	FLOAT	FLOAT
SPLIT	2	V+	UNLOCK
TAYLOR	3	V−	UNLOCK
TIME-OUT	4	FLOAT	V−

TYPICAL PERFORMANCE CHARACTERISTICS

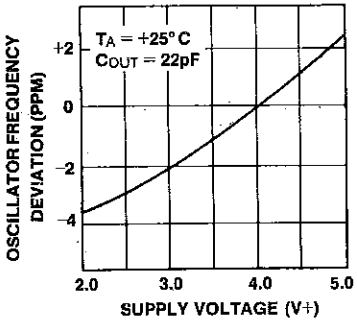
SUPPLY CURRENT VS VOLTAGE



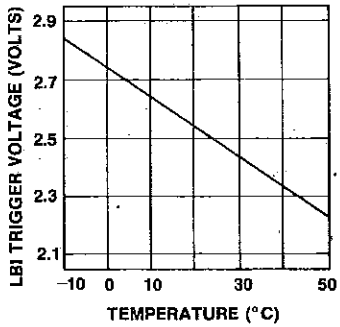
SEGMENT CURRENT VS SUPPLY VOLTAGE



OSC. STABILITY VS SUPPLY VOLTAGE



LOW BATTERY INDICATOR (LBI) TRIGGER VOLTAGE VS TEMPERATURE



7

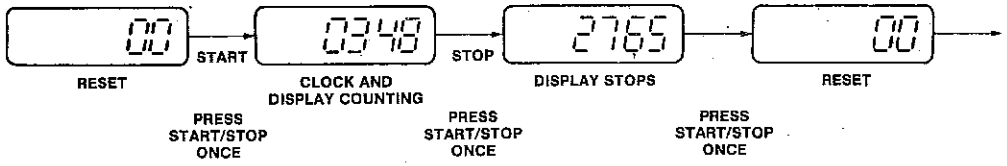
FUNCTIONAL OPERATION

Turning on the stopwatch will bring up the reset state with the fractional seconds displaying 00 and the other digits blanked. This display always indicates that the stopwatch is ready to go.

The display can be turned off in any mode by connecting the chip enable input to V+.

START/STOP/RESET MODE

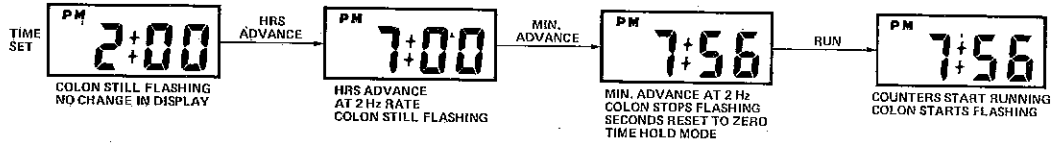
When the mode input is floating and the display input is floating or connected to V+ the circuit is in the start/stop/reset mode.



The start/stop/reset mode can be used for single event timing in a one-button stopwatch; an additional switch can be used to provide an instant reset. To time another event, the display must be reset before the start of the event.

one minute. The range of the stopwatch is 59 minutes 59.99 seconds, and if an event exceeds one hour, the number of hours must be remembered by the user. Leading zeroes are not blanked after one hour.

TIME SETTING

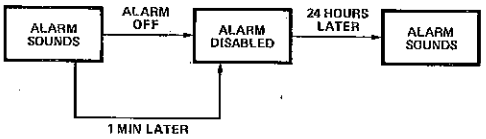


NOTE: When the HRS/MIN Advance input is activated there will be a pause of less than one second before the counters start advancing at a 2 Hz rate.

TIME SETTING

To set the time, the RUN/SET switch is placed in the Time Set position, and the HRS/MIN advance input is used to advance the hours or minutes. The seconds are reset to zero and counting is stopped whenever the minutes are set. The clock will start when the RUN/SET switch is put back into the RUN position, and while in the RUN position, inputs from the HRS/MIN advance switch are disabled to prevent accidental setting.

ALARM OPERATION



7

The alarm comparator provides a 24 hour alarm in both 12 and 24 hour modes. When the time of day and alarm times are equal, the alarm outputs are enabled, providing that the ALARM OFF input is at V_T^-. If the ALARM OFF input is at V^+, the alarm outputs will not be enabled. The alarm outputs provide a push-pull, or bridge, configuration for direct drive of a piezoelectric transducer, and if increased drive (loudness) is desired, a coil and external NPN transistor may be used. The external transistor should be driven by the ALARM 1 output. The coil DC resistance should be 100Ω or greater, to limit the peak current to less than 13 mA.

The alarm signal is a complex waveform that generates the Intersil Cricket sound. The alarm output will automatically stop after one minute unless either the ALARM OFF or the SNOOZE input is used. The alarm transducer should be selected to provide maximum output (loudness) at 4 kHz, that is, it should be resonant at 4 kHz.

SNOOZE OPERATION

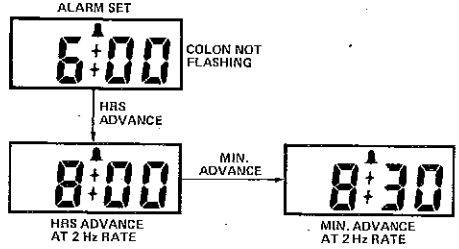
A momentary closure of the SNOOZE switch to V^+ will silence the alarm and start the snooze timer. The Snooze input must be activated during the one minute

After 8 minutes the alarm will again sound, and will continue for 2 minutes and stop unless ALARM OFF is used or another Snooze cycle is activated. The Snooze may be repeated as many times as desired.

NOTE: In die form, all the SNOOZE input pads are available, allowing the manufacturer or user to select snooze times from 2 to 14 minutes in 2 minute steps. These pads are identified as SN1, SN2 and SN3. See the following table for the selection of Snooze times:

INPUT CODE (1 = V^+)			SNOOZE TIME
SN3	SN2	SN1	
0	0	0	None
0	0	1	2 minutes
0	1	0	4 minutes
0	1	1	6 minutes
1	0	0	8 minutes
1	0	1	10 minutes
1	1	0	12 minutes
1	1	1	14 minutes

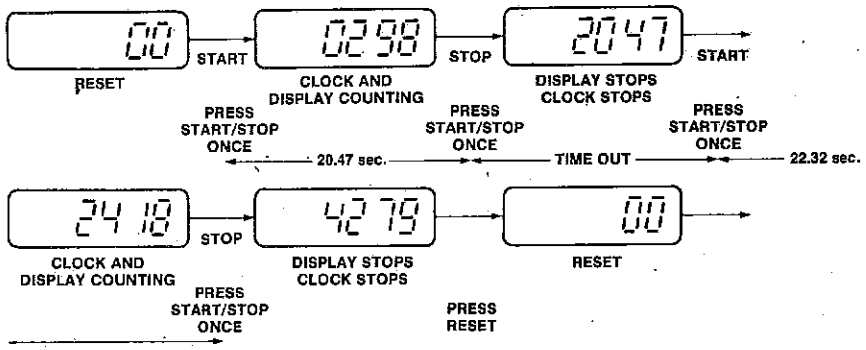
ALARM SETTING



The alarm time is set by switching to Alarm Set, then using the HRS/MIN ADVANCE input to set hours and minutes. The alarm time is displayed only when the

TIME OUT MODE

When the mode input is floating and the display input is tied to V-, the stopwatch is in the time-out mode.



In the time-out mode the clock and display alternately start and stop with activations of the start/stop switch. Reset can be used at any time. The display unlock button is bypassed in this mode.

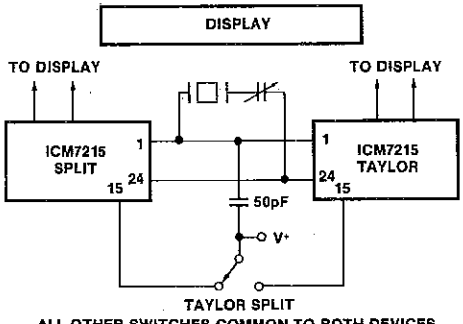
APPLICATION NOTES

LOW BATTERY INDICATOR

The on-chip low battery indicator is intended for use with a small LED or the decimal points on a standard LED display. The output is the drain of a p-channel transistor two-thirds the size of the segment drivers, and designed to provide a trigger voltage of approximately 2.5 volts at room temperature. Normal AA type batteries will provide many hours of accurate timekeeping after the indicator comes on, however the wide voltage spread between the LBI voltage and minimum operating voltage is required to guarantee low battery indication under worst case conditions.

CHIP ENABLE

The chip enable input is used to disable both segment and digit drivers without affecting any of the functions of the device. When the chip enable input is floating or connected to V-, the display is enabled, and when the tied to V+ the display is turned off. One example of the many possible uses of this feature is driving one display from two ICM7215 devices, one in the split mode and the other in the taylor mode. The circuit below indicates how the user can obtain lap and cumulative readings of the same event.



ALL OTHER SWITCHES COMMON TO BOTH DEVICES

SWITCH CHARACTERISTICS

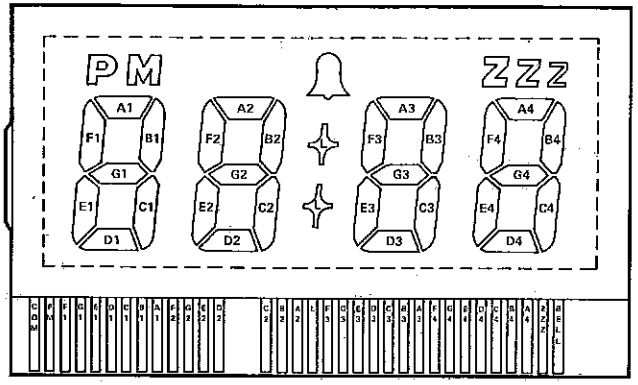
The ICM7215 is designed for use with SPST switches throughout. On the display unlock and reset inputs the characteristics of the switches are unimportant, since the circuit responds to a logic level held for any length of time however short. Switch bounce on these inputs does not need to be specified. The start/stop input, however, responds to an edge and so requires a switch with less than 15ms of switch bounce. The bounce protection circuitry has been specifically designed to let the circuit respond to the first edge of the signal, so as to preserve the full accuracy of the system.

LATCHUP CONSIDERATIONS

Due to the inherent structure of junction isolated CMOS devices, the circuit can be put in a latchup mode if large currents are injected into device inputs or outputs. For this reason special care should be taken in a system with multiple power supplies to prevent voltages being applied to inputs and/or outputs before power is applied to the 7215. If only inputs are affected, latchup can also be prevented by limiting the current into the input terminal to less than 1mA.

DISPLAY

MOTOROLA	MLC4D5
BECKMAN	737-01
LADCOR	LAD-001
HAMLIN	3411
TIMEX	T1001
COCKROFT	CII202

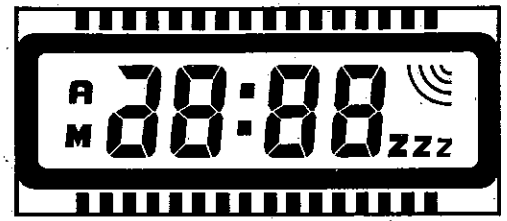


DISPLAY FONT

NUMBERS

1 2 3 4 5 6 7 8 9 0

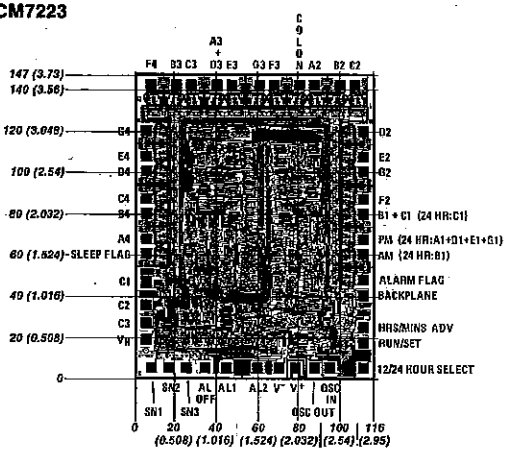
COCKROFT CII201



7

CHIP TOPOGRAPHY

ICM7223



CHIP DIMENSIONS: 116 x 147 mils (2.95 x 3.73 mm)

ICM7223
4-Digit LCD Clock Circuit with Snooze Alarm

FEATURES

- 3-1/2 or 4 digit display with AM/PM and alarm flags
- 12/24 hour user selectable formats
- Direct alarm drive @ 3V p-p, with complex (cricket) alarm tone
- 8 minute snooze (Dice programmable from 2 to 14 minutes in two minute increments)
- Single battery operation (1.5V)
- Low current — 6 μA maximum
- On-chip fixed oscillator input capacitor
- 32 kHz oscillator requires only quartz crystal and trimming capacitor
- Voltage tripler for large displays

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7223IPL	-20°C to +70°C	40 Pin Plastic DIP
ICM7223D/D	-20°C to +70°C	DICE

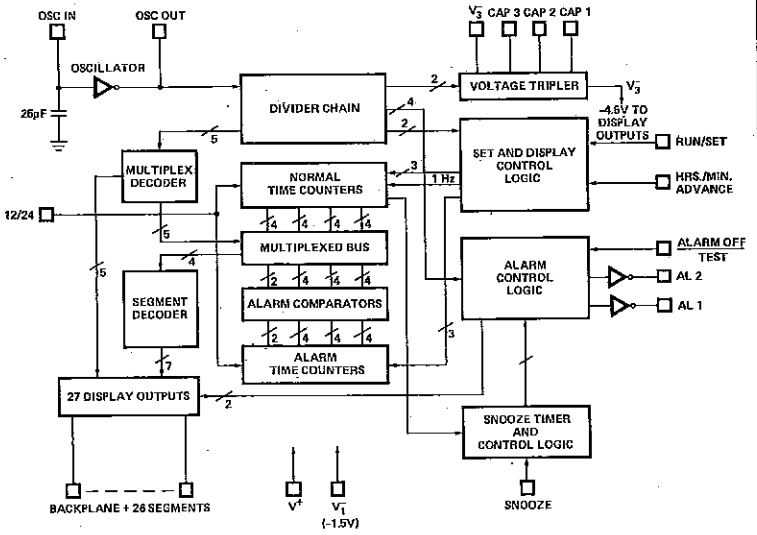
GENERAL DESCRIPTION

The ICM7223 is a fully integrated 4-digit LCD clock circuit with 24 hour alarm and 8 minute snooze timer. For high accuracy and low power consumption a 32.768 KHz quartz watch crystal is used as the time base, and the number of external components has been reduced to a minimum.

The time keeping and alarm time counters are split during setting, allowing hours and minutes to be set independently, each at a 2 Hz rate. A 'time hold' mode is entered when setting minutes; seconds are automatically reset to zero. The clock starts when the RUN mode is entered, thereby permitting synchronization of the clock to the nearest second. Seconds are not displayed.

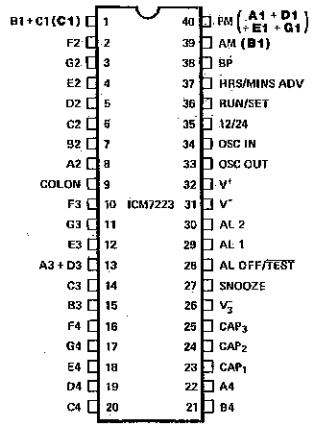
The ICM7223 is fabricated using Intersil's low threshold metal gate CMOS process for minimum cost and long battery life.

BLOCK DIAGRAM



PIN CONFIGURATION

(OUTLINE DRAWING PL)

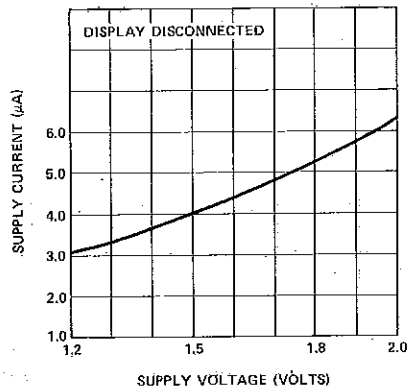


PARENTHESES AND **BOLD TYPE** INDICATE 24 HOUR OPERATION

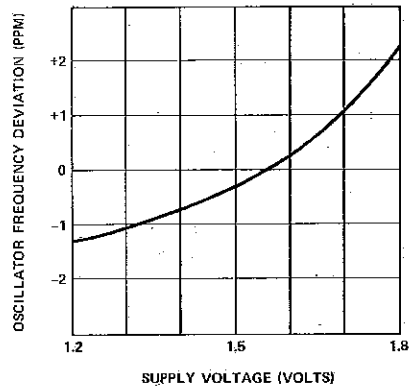
7

TYPICAL PERFORMANCE CHARACTERISTICS

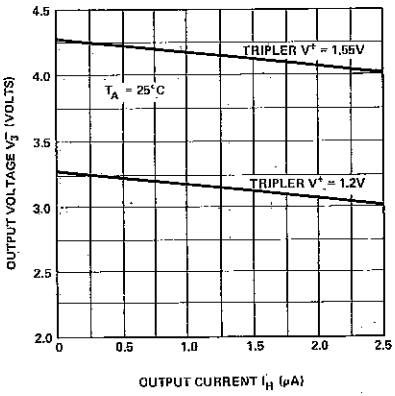
SUPPLY CURRENT VS. SUPPLY VOLTAGE



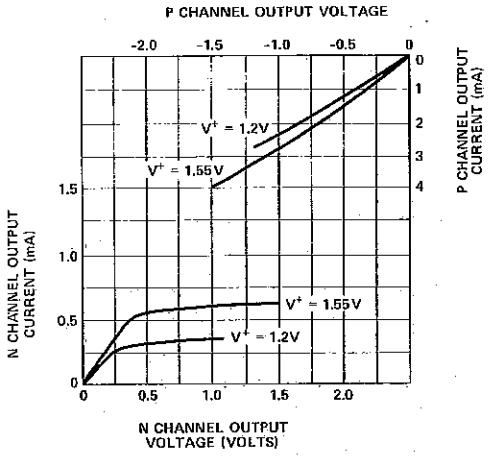
OSCILLATOR STABILITY VS. SUPPLY VOLTAGE



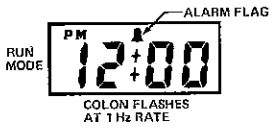
VOLTAGE MULTIPLIER OUTPUT VOLTAGE VS. OUTPUT CURRENT



ALARM DRIVER OUTPUT CURRENT VS. OUTPUT VOLTAGE

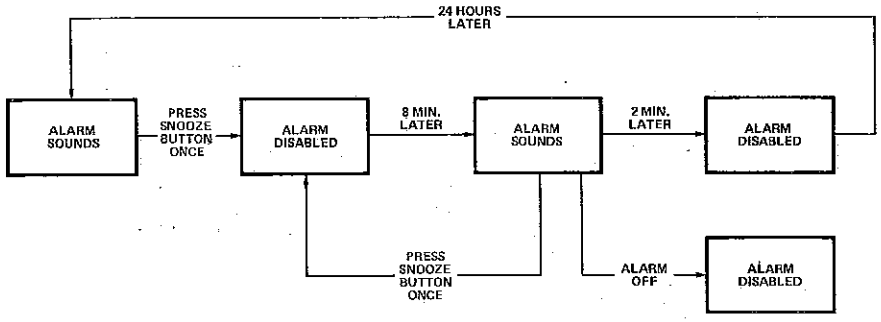


NORMAL CLOCK OPERATION



In normal operation, hours and minutes are displayed with the colon flashing at a 1 Hz rate. An AM and a PM indicator flag is provided in the 12 hour mode, while in the 24 hour mode, the pads used for the AM/PM flags are utilized to drive the segments which produce the numeral "2" in the tens of hours digit. The alarm flag will be on if the alarm is enabled, and off if the alarm is not enabled; (Alarm Off input at V^+).

SNOOZE OPERATION



NOTE: IF ALARM OFF IS LEFT AT V^+ THE ALARM WILL NOT SOUND 24 HOURS LATER.

APPLICATION NOTES

ALARM DRIVE

The ICM7223 alarm output transistors are capable of directly driving a piezoelectric ceramic transducer at 3 volts peak-to-peak. Any transducer that does not require more than 1 mA of peak current may also be used. The transducer should generate maximum output at 4 kHz. If a louder sound is desired, buffering (using an NPN transistor and 5 mho coil) or sound enhancement techniques such as a resonant cavity or diaphragm will be required. See Application Bulletin A031 for details.

TEST MODE

The high speed test mode for automatic testing is entered by pulling the ALARM OFF/TEST input to -7 volts referenced to V_T. In this state the HRS/MIN ADVANCE input will advance the appropriate counters at the rate that the input is toggled. The colon will appear to stop flashing as it is changing state more rapidly than the display can respond. In the run mode the minutes will change at a 4.27 Hz rate, as the clock has been speeded up by a factor of 256 Hz. The backplane frequency will be 512 Hz. The voltage tripler drive frequencies remain the same as in normal modes.

ALARM AND DISPLAY TEST

If the ALARM OFF and SNOOZE buttons are pushed simultaneously, all segments of the display will be turned on and the alarm will sound, while none of the time counter contents are disturbed.

VOLTAGE MULTIPLIER

The ICM7223 voltage multiplier may be utilized only in a tripler configuration; only four pins, and three external capacitors are required. The connection of the capacitors differs from that used in standard watch circuit type voltage multipliers, therefore close attention should be paid to substrate design to ensure the proper connection of the capacitors.

OSCILLATOR

The oscillator of the ICM7223 is designed for low frequency operation at very low currents from a 1.55 volt supply. The oscillator is of the inverter type with a nonlinear feedback resistor included on chip, which has a maximum resistance under startup conditions. The nominal load capacitance of the crystal should be less than 15 pF, typically 12 pF. In specifying the crystal, the motional capacitance, series resistance and tuning tolerance have to be compatible with the characteristics of the circuit to insure startup and operation over a wide voltage range under worst case conditions.

The following expressions can be used to arrive at a crystal specification:

Tuning range

$$\frac{\Delta f}{f} = \frac{C_m}{2\,(C_O + C_L)}\ ;\ C_L = \frac{C_{IN}\,C_{OUT}}{C_{IN} + C_{OUT}}$$

g_m required for startup

$$g_m = 4\pi^2 f^2\, C_{IN}\, C_{OUT}\, R_S \left(1 + \frac{C_O}{C_L}\right)^2$$

where

R_S = Series Resistance of Crystal
f = Frequency of the Crystal
Δf = Frequency Shift from Series Resonance Frequency
C_O = Static Capacitance of Crystal
C_{IN} = Input Capacitance
C_{OUT} = Output Capacitance
C_L = Load Capacitance of Crystal
C_m = Motional Capacitance of Crystal

The g_m required for startup calculated should not exceed 50% of the g_m guaranteed for the device.

POWER UP RESET

An on chip circuit is provided that will reset all counters and flip-flops to a known state when power is first applied. The alarm and timekeeping counters will be reset to 1:00 am in the 12 hr. mode and 0:00 in the 24 hr. mode. This function is not tested during automatic testing, as it does not affect normal circuit operation.

7

ICM7223A 3-1/2 Digit LCD Battery Operated Clock Circuit With Snooze and Sleep Timers

FEATURES

- Single 9V transistor battery operation
- 3-1/2 digit display with AM/PM, SLEEP and ALARM flags
- Direct alarm drive with complex (cricket) alarm tone
- Programmable snooze
- Programmable sleep timer with RADIO ENABLE OUTPUT
- Wide operating voltage range — 4 to 15 volts
- Low current — 15μA @ 9V
- On-chip fixed oscillator input capacitor
- Uses standard 32.768 KHz crystal
- Low battery indicator (display flashes at 1 Hz)
- Display and alarm test

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7223AIPL	-20°C to +85°C	40 Pin Plastic DIP
ICM7223A/D	-20°C to +85°C	DICE

GENERAL DESCRIPTION

The ICM7223A is a fully integrated 3-1/2 digit LCD clock circuit with 24 hour alarm, and sleep and snooze timers. For high accuracy and low power consumption a 32.768 kHz quartz watch crystal is used as the time base, while the number of external components has been reduced to a minimum. This circuit is intended for use in 9V clock-radio systems where both the clock and the radio operate from the same battery.

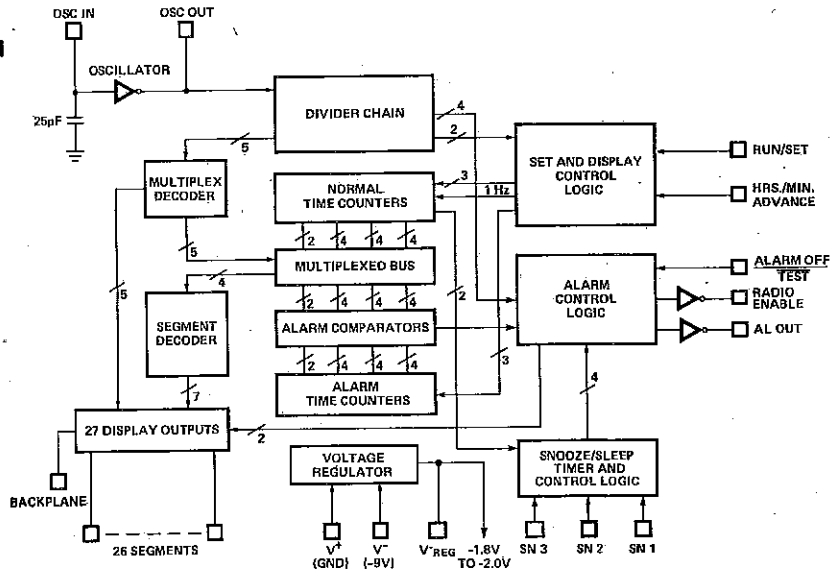
The time keeping and alarm time counters are split during setting, allowing hours and minutes to be set independently, each at a 2 Hz rate. A 'time hold' mode is entered when setting minutes; seconds are automatically reset to zero. The clock starts when the RUN mode is entered; this permits synchronization of the clock to the nearest second. Seconds are not displayed.

The alarm employs a snooze timer that may be programmed from 2 to 14 minutes in two minute increments; the sleep timer may be set from 8 to 56 minutes in 8 minute increments. The alarm outputs consist of a complex (cricket) alarm tone to directly drive a speaker of piezoelectric transducer, and a radio enable output which allows control of a clock radio. Low battery voltage is indicated by the display flashing at a 1 Hz rate whenever the battery voltage falls below about 5.6V.

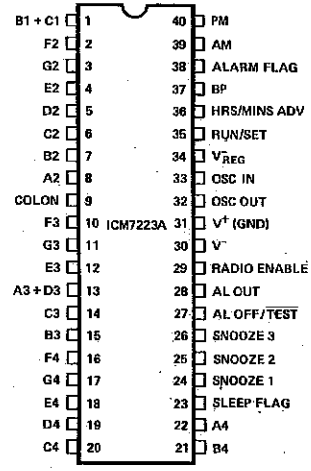
The ICM7223A is fabricated using Intersil's low threshold metal gate CMOS process for minimum cost and long battery life. Current drain at 9 volts is typically 15μA with a maximum of 25μA.

7

BLOCK DIAGRAM



PIN CONFIGURATION (outline dwg PL)



NOTE: CONSULT FACTORY IF 24 HOUR TIME DISPLAY IS DESIRED.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -20°C to +85°C
Power Dissipation[1] ..... 500 mW
Supply Voltage 18V
Input Voltage
(OSC IN, SN_1, SN_2, SN_3) ..... $-2V \le V_{IN} \le V^+ + 0.3V$
(RUN/SET, HRS/MIN ADV, AL OFF/TEST) ..... $V^- - 0.3V \le V_{IN} \le V^+ + 0.3V$
Output Voltage
(OSC OUT) ..... $-2V \le V_{OUT} \le V^+$
(AL OUT, RADIO ENABLE, All Segment Drivers) ..... $V^- \le V_{OUT} \le V^+$

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

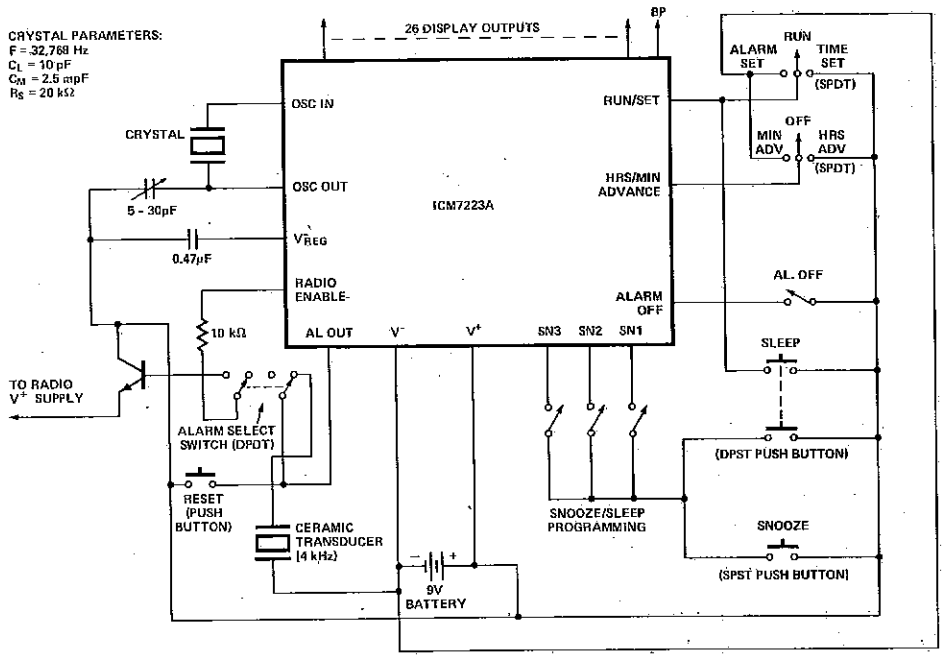
OPERATING CHARACTERISTICS

All testing at 25°C; All numbers stated in absolute value; $V^+ = 9V$ unless otherwise specified.

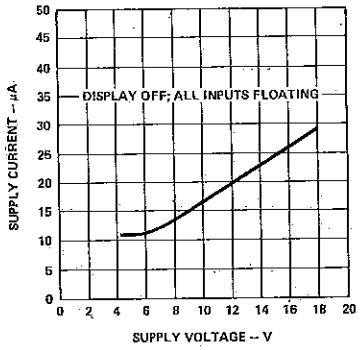
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
Supply Voltage Range Timekeeping Accurate	V^+		4		18	V
Supply Current	1^+	$V^+ = 9V$		15	25	μA
Oscillator Input Current(3)	I_{OSCI}	'OSC IN' Connected to V^+ 'OSC OUT' Open Circuit		0.2		μA
Oscillator Input Capacitance	C_{IN}		20	25	30	pF
Oscillator Transconductance	g_m		10	15		μmho
Oscillator Stability	f_{STAB}	$5V \le V_{SUPPLY} \le 15V$		0.7	1.0	ppm
Alarm Saturation Resistance	$R_{AL(on)}$	P-ch at 10mA		220	300	Ω
		N-ch at 10 mA		100	150	Ω
Segment Drive Current	I_{SEG}	$V_{SAT} = 0.2V$ (Both Directions)	5			μA
Backplane Drive Current	I_{BP}	$V_{SAT} = 0.1V$ (Both Directions)	20			μA
Switch Actuation Current	I_{SW}	$V_{SW} = V^+$		10	30	μA
		$V_{SW} = V^-$		10	30	μA

NOTES: 1. This value of power dissipation is that of the package and will not be obtained under normal operating conditions.

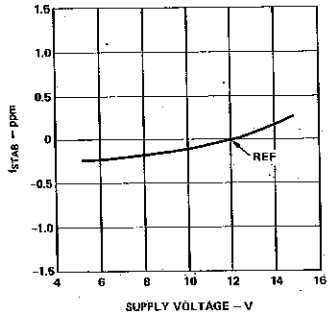
TYPICAL CLOCK RADIO APPLICATION



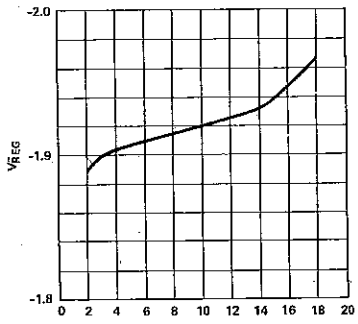
SUPPLY CURRENT vs. SUPPLY VOLTAGE



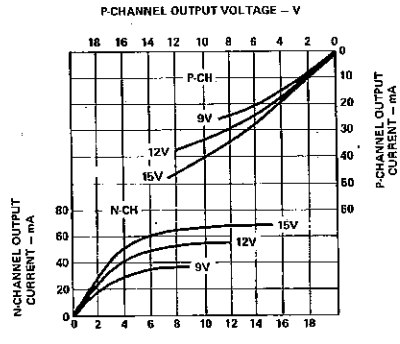
OSCILLATOR STABILITY vs. SUPPLY VOLTAGE



VOLTAGE REGULATOR OUTPUT vs. SUPPLY VOLTAGE

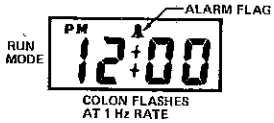


ALARM DRIVER OUTPUT CURRENT vs. OUTPUT VOLTAGE



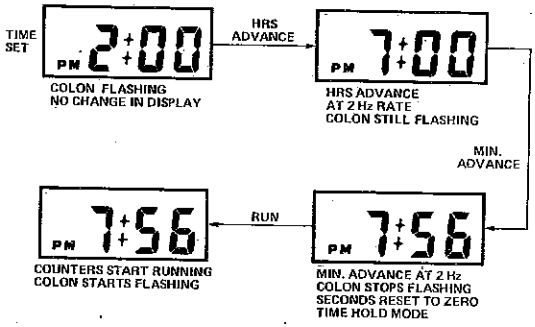
NORMAL CLOCK OPERATION

In normal operation hours and minutes are displayed with the colon flashing at a 1 Hz rate. AM and PM indicators are provided. The alarm flag will be on if the ALARM OFF input is at V^-, and off with the ALARM OFF input at V^+. Time is displayed in a 12 hour format with AM/PM annunciators.



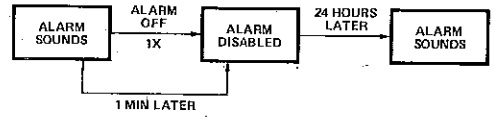
TIME SETTING

To set the time, the RUN/SET switch is placed in the Time Set position, and the HRS/MIN advance input is used to advance the hours or minutes. The seconds are reset to zero and counting is stopped whenever the minutes are set. The clock will start when the RUN/SET switch is put back into the RUN position, and while in the RUN position, inputs from the HRS/MIN advance switch are disabled to prevent accidental setting.



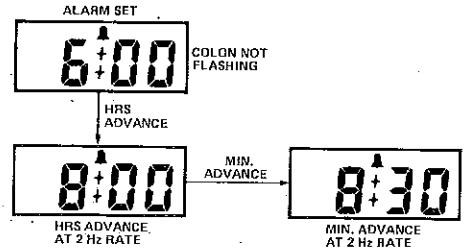
NOTE: When the HRS/MIN Advance input is activated there will be a pause of less than one second before the counters start advancing at a 2 Hz rate.

ALARM OPERATION



The alarm comparator provides a 24 hour alarm by taking into account AM and PM. When the time of day and alarm times agree, and the ALARM OFF input is floating, the ALARM and RADIO ENABLE outputs are activated; the alarm sounds and the RADIO ENABLE line goes to V^+. Momentarily tying the ALARM OFF input to V^+ will silence both the alarm and the radio. The alarm will automatically shut off after one minute if ALARM OFF is not used; the RADIO ENABLE will stay HIGH until either the ALARM OFF or SNOOZE inputs are used. The SNOOZE input must be applied within one minute in order to begin a snooze,cycle.

ALARM SETTING

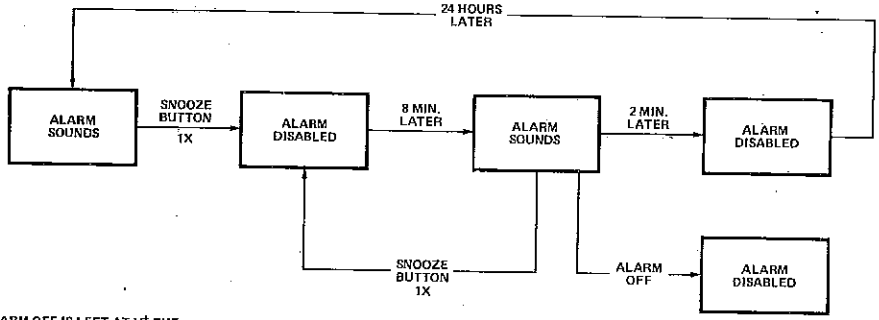


The alarm time is set by switching to Alarm Set, then using the HRS/MIN ADVANCE input to set hours and minutes. The alarm time is displayed only when the RUN/SET switch is in the Alarm Set position.

SNOOZE OPERATION

To begin a snooze cycle, the SNOOZE input must be momentarily shorted to V^+ during the one minute that the alarm is sounding or the RADIO ENABLE line is high. When this is done the alarm will be silenced and the snooze timer started; the alarm will sound again after the selected snooze time. Unless the ALARM OFF input is used, the alarm will automatically shut off after two

SNOOZE OPERATION



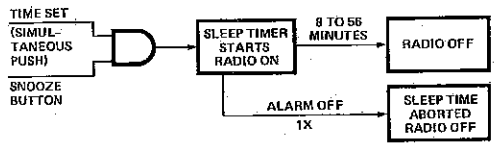
NOTE: IF ALARM OFF IS LEFT AT V^+ THE ALARM WILL NOT SOUND 24 HOURS LATER.

minutes. The RADIO ENABLE will remain on until the ALARM OFF line is activated, however, a second snooze cycle can be initiated with the SNOOZE switch. This can only be done if the SNOOZE is activated while the alarm is sounding.

The snooze times are programmable in 7 steps from 2 to 14 minutes. Programming is accomplished with binary coding on the three SNOOZE inputs, as shown in the following table:

INPUT CODE (1 = V⁺)			SNOOZE TIME	SLEEP TIME
SN3	SN2	SN1		
0	0	0	None	None
0	0	1	2 minutes	8 minutes
0	1	0	4 minutes	16 minutes
0	1	1	6 minutes	24 minutes
1	0	0	8 minutes	32 minutes
1	0	1	10 minutes	40 minutes
1	1	0	12 minutes	48 minutes
1	1	1	14 minutes	56 minutes

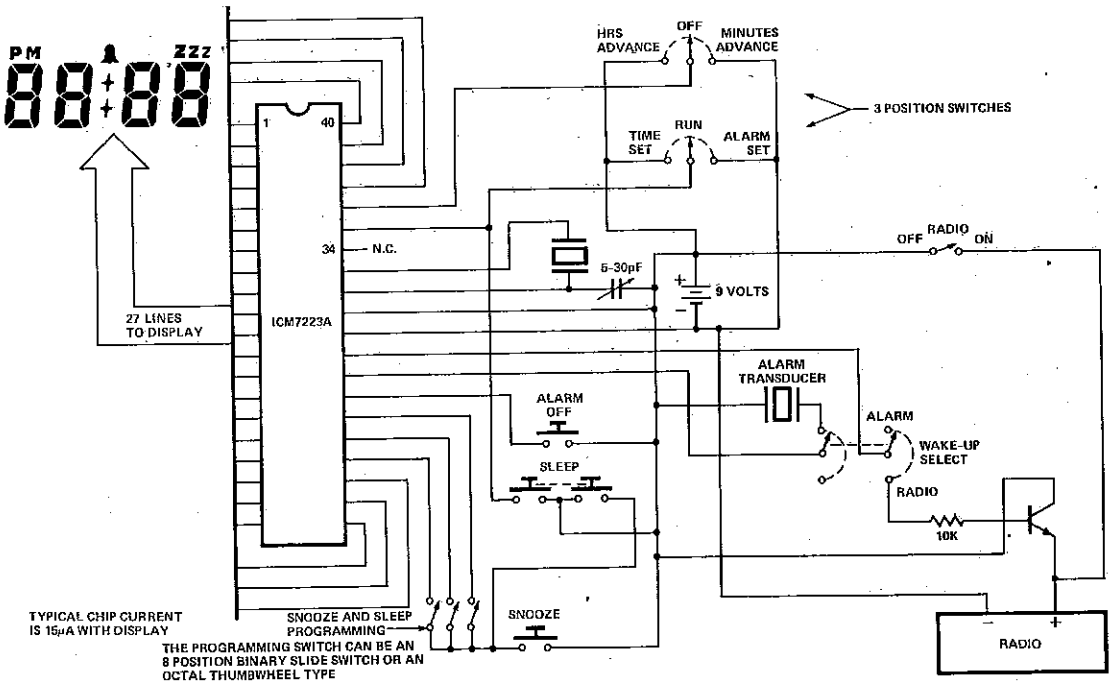
SLEEP TIMER OPERATION



The sleep timer may be activated at any time except during a snooze cycle or when the alarm is sounding. The sleep timer is started by setting the RUN/SET switch in the SET position and momentarily activating the SNOOZE switch. Sleep times are programmed with the snooze inputs; see table on previous page.

Another method for sleep timer activation is to use a single DPST pushbutton switch, with one pole connected to the RUN/SET switch and the other to the common side of the SNOOZE programming switch. The other side of the switches is tied to V^+. (See typical application, page 3). This method allows the use of a "dedicated" sleep button, which may be recessed to prevent accidental activation.

When the sleep timer is activated the RADIO ENABLE output is set high to turn on a radio and the sleep flag appears on the display. At the end of the programmed sleep time the RADIO ENABLE output is returned to V^- and the sleep flag disappears.



ICM7223A 12HR LCD SNOOZE ALARM CLOCK RADIO CIRCUIT WITH SLEEP TIMER.
(9 volt single battery operation)

LOW BATTERY INDICATION

The ICM7223A is provided with a completely integrated low battery indicator. When the supply voltage drops below about 5.6V the display will begin flashing at a 1 Hz rate. Actual trigger points vary from chip to chip, but will usually be in the range of 5.2V to 6V. Time keeping will not be affected.

CHIP RESET

Power up reset is not provided on the 7223A, as interaction between the V^+ and V^- inputs and the voltage regulator in noisy environments could cause spurious resetting. Resetting the circuit to a known state, 1:00 AM, can be accomplished by momentarily connecting the ALARM OUT output to V^+; this can be done with a NO SPST switch. This same method may be employed to clear the 7223A in the event that it powers up in an illegal state. The switch should be made accessible to the user for use when changing batteries.

TEST MODE OPERATION

This mode, provided for high speed automatic testing, is entered by shorting ALARM OFF to V^-. The minutes will then advance at a 4.27 Hz rate and setting can be accomplished by the application of a digital input to the hrs — mins advance input. The counter will then advance once per pulse. Note that in the test mode there is no debounce protection on the HRS/MINS ADVANCE input.

ALARM AND DISPLAY TEST

If the ALARM OFF and SNOOZE buttons are pushed simultaneously, all segments of the display will be turned on and the alarm will sound, while none of the time counter contents are disturbed.

OSCILLATOR

The oscillator of the ICM7223A is designed for low frequency operation at very low currents from a 9 volt supply. The oscillator is of the inverter type with a nonlinear feedback resistor included on chip, which has a maximum resistance under startup conditions. The nominal load capacitance of the crystal should be less than 15 pF, typically 12 pF. In specifying the crystal, the motional capacitance, series resistance and tuning tolerance have to be compatible with the characteristics of the circuit to insure startup and operation over a wide voltage range under worst case conditions.

The following expressions can be used to arrive at a crystal specification:

Tuning range

$$\frac{\Delta f}{f} = \frac{C_m}{2(C_O + C_L)} \; ; \; C_L = \frac{C_{IN}\, C_{OUT}}{C_{IN} + C_{OUT}}$$

g_m required for startup

$$g_m = 4\pi^2 f^2\, C_{IN}\, C_{OUT}\, R_S \left(1 + \frac{C_O}{C_L}\right)^2$$

where

R_S	=	Series Resistance of Crystal
f	=	Frequency of the Crystal
Δf	=	Frequency Shift from Series Resonance Frequency
C_O	=	Static Capacitance of Crystal
C_{IN}	=	Input Capacitance
C_{OUT}	=	Output Capacitance
C_L	=	Load Capacitance of Crystal
C_m	=	Motional Capacitance of Crystal

The (calculated) g_m required for startup should not exceed 50% of the g_m guaranteed for the device.

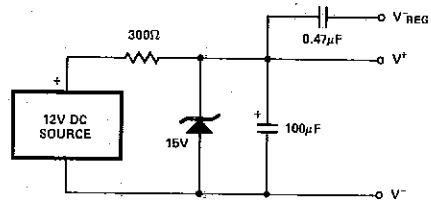
ALARM DRIVE

The ICM7223A will directly drive any suitable audio transducer (piezoelectric ceramic, or magnetic speaker) with a peak frequency response of 4 kHz with $V^+ = 9V$ and a peak current of 10 mA. The volume should be more than adequate; no buffering should be required.

POWER SUPPLY CONSIDERATIONS

The ICM7223A contains an on-chip CMOS voltage regulator which operates all timing and counting logic circuitry at about 1.8 to 2.0V below V^+. This provides low current operation over a voltage range of 4-15V and also improves oscillator stability. The LCD maximum operating voltage will be the limiting factor in most cases, therefore the supply voltage will rarely exceed 12V.

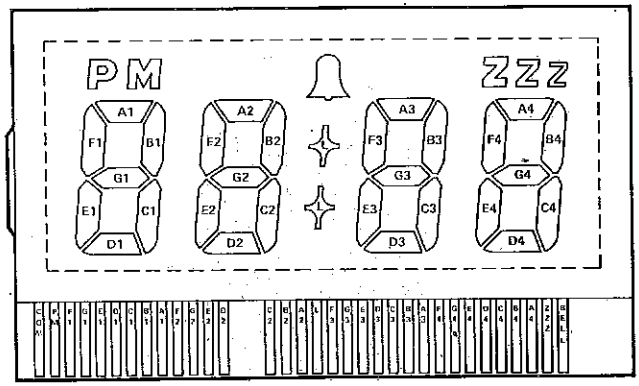
For applications which involve power supplies with high noise levels or transients, it will be necessary to provide supply filtering. The voltage regulator output (V^-_{REG}) should be decoupled to V^+ with a 0.22μF to 0.47μF capacitor, and the V^+ and V^- lines should be low-pass-filtered using a 300Ω resistor and 100μF capacitor. Note that a zener diode in parallel with the filter cap will limit voltage spikes to 15V, and should be included if the common "24V survival" required for automotive use is desired.



ICM7223A

DISPLAY

MOTOROLA	MLC406
BECKMAN	737-01
LADCOR	LAD-001
HAMLIN	3411
TIMEX	T1001
COCKROFT	CII202

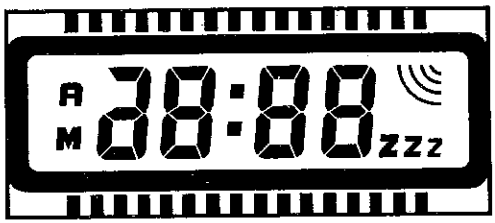


DISPLAY FONT

NUMBERS

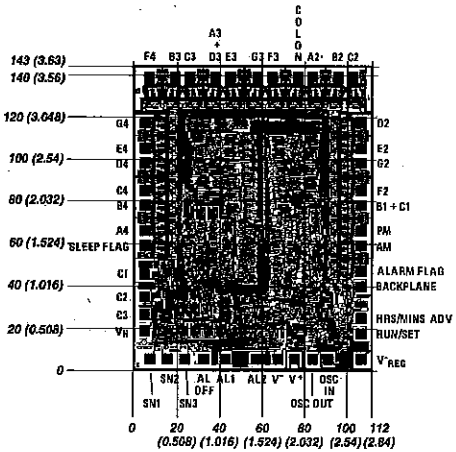
1 2 3 4 5 6 7 8 9 0

COCKROFT CII201



CHIP TOPOGRAPHY

ICM7223A



CHIP DIMENSIONS: 112 x 143 mils (2.84 x 3.63 mm)

ICM7241 CMOS Frequency Divider 4.19 MHz to 32 kHz

FEATURES

- **Single battery operation (1.2 - 1.8V)**
- **Low power consumption — typ. 40μA @ 1.5V**
- **Oscillator biasing resistor included on-chip**

GENERAL DESCRIPTION

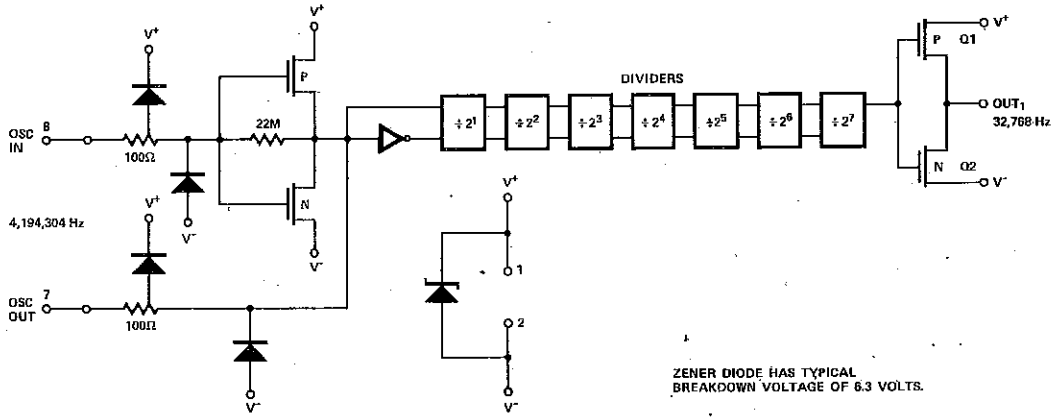
The ICM7241 is a fully integrated oscillator, 2 divider and output driver which efficiency converts 4.194304 MHz to 32.768kHz using a minimum of power. Only three external components are necessary for complete oscillator operation; a 4.194304 MHz crystal, a fixed input capacitor, and an output trimmer capacitor. The output has a low enough impedance to satisfy most drive requirements.

ABSOLUTE MAXIMUM RATINGS

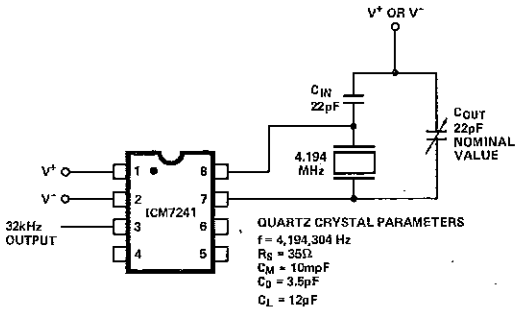
Power Dissipation Output Short Circuit[2] . 300 mW
Supply Voltage 3V
Output Voltage[1]
Input Voltage[1]
Storage Temperature ..... -30°C to +125°C
Operating Temperature ..... -20°C to 70°C

NOTES:
1. Except for instantaneous static discharges all terminals may exceed the supply voltage (2.0V max) by ±0.5 volt provided that the currents in these terminals are limited to 2 mA each.
2. This value of power dissipation refers to that of the package and will not be obtained under normal operating conditions.

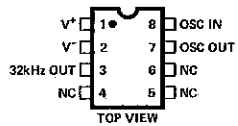
SCHEMATIC DIAGRAM



TYPICAL CONNECTION



PIN CONFIGURATION (outline dwg PA)



PIN 1 IS DESIGNATED BY EITHER A DOT OR A NOTCH.

ORDERING INFORMATION

Order devices by following part number: ICM7241

7

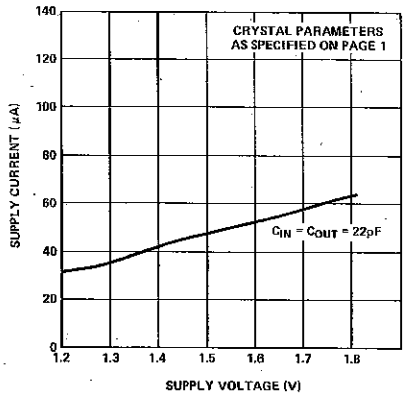
TYPICAL OPERATING CHARACTERISTICS

V^+ = 1.5V, fosc = 4,194,304 Hz, T_A = 25°C, unless otherwise specified. All numbers in absolute values.

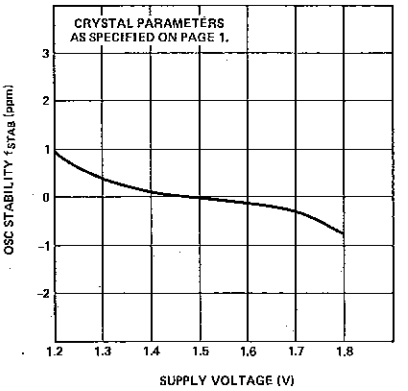
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Current	I^+			40	70	µA
Guaranteed Operating Voltage Range	V^+	-20°C ≤ to ≤ 70°C	1.2		1.8	V
P-Ch Output Saturation Resistance	R_{SAT}	I_{OUT} = .5mA		680	2	kΩ
N-Ch Output Saturation Resistance	R_{SAT}	I_{OUT} = .5mA		240	1	kΩ
Oscillator Stability	f_{STAB}	1.2V < V^+ < 1.6V C_{IN} = C_{OUT} = 15pF		1		ppm
Oscillator Start-Up Time	t_{start}	V^+ = 1.2V			1.0	sec

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

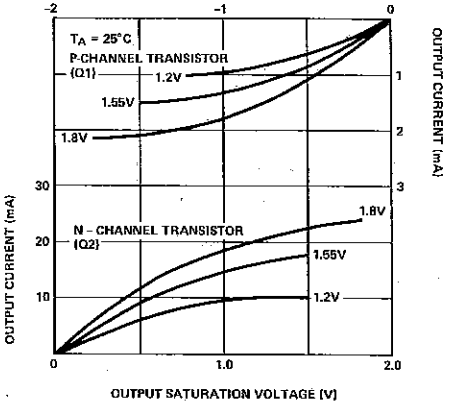
SUPPLY CURRENT vs. SUPPLY VOLTAGE



OSCILLATOR STABILITY vs. SUPPLY VOLTAGE



OUTPUT CURRENT (SOURCE) vs. OUTPUT SATURATION VOLTAGE



ICM7245 Quartz Analog Watch Circuit

FEATURES

- **Very low current consumption: 0.4μA at 1.55 volt typical**
- **32 kHz oscillator requires only quartz crystal and trimming capacitor**
- **Bipolar stepper drive with low output ON resistance: 200 ohms maximum (7245 A/B/D/E/F)**
- **Unipolar stepper drive with very low output ON resistance: 50 ohms maximum (7245U)**
- **Extremely accurate: oscillator stability typically 0.1 ppm**
- **STOP function for easy time synchronization**
- **TEST input for highspeed testing**
- **Wide temperature range: -20° C to +70° C**
- **On chip fixed oscillator capacitor: 20pF ±20%**

TABLE OF OPTIONS

Device Number	Bipolar/ Unipolar	Pulse Width (ms)	Pulse Frequency	Oscillator Capacitor
ICM7245A	B	9.7	1Hz	C_{OUT}
ICM7245B	B	7.8	1Hz	C_{IN}
ICM7245D	B	7.8	0.1Hz (1 pulse/ 10 seconds)	C_{OUT}
ICM7245E	B	7.8	0.0833Hz (1 pulse/ 12 seconds)	C_{IN}
ICM7245F	B	7.8	0.05Hz (1 pulse/ 20 seconds)	C_{IN}
ICM7245U	U	3.9	1Hz	C_{IN}

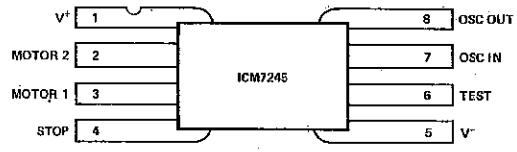
GENERAL DESCRIPTION

The ICM7245 is a very low current, low voltage microcircuit for use in analog watches. It consists of an oscillator, dividers, logic and drivers necessary to provide either bipolar or unipolar drive for minimum-component count watches. The oscillator is extremely stable over wide ranges of voltage and temperature, and thus combines high accuracy with low system power. The ICM7245 is fabricated using Intersil's low threshold metal-gate CMOS process.

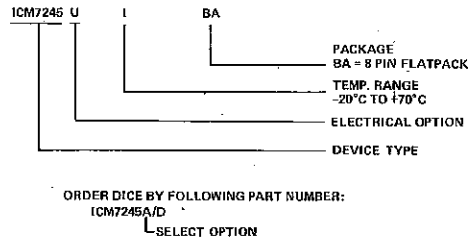
The inverter oscillator contains all components on-chip except for the tuning capacitor and quartz crystal. The binary divider consists of 15 stages, the last 5 of which may be reset. If a reset (stop) occurs during an output pulse, the duration of the pulse is not affected. When the reset is released, the first output occurs approximately 1 second later. For the bipolar version, memory reset logic is included to make sure the first pulse after a "stop" occurs on the opposite output from the one just before the "stop".

The bipolar bridge output consists of two large inverters, normally high. The output ON resistance of the P and N channel devices in series is 200Ω maximum @ 1 mA. In unipolar operation, the output is made up of a single normally high inverter. The ON resistance of the N-channel device is 50Ω maximum @ 3 mA.

PIN CONFIGURATION (OUTLINE DRAWING BA)



ORDERING INFORMATION



7

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... -40°C to +125°C
Operating Temperature ..... -20°C to +70°C
Power Dissipation (Note 1) ..... 25 mW
Supply Voltage ($V^+ - V^-$) ..... 3.0 volts
Lead Temperature (Soldering, 10 sec) ..... 300°C
Input Voltages ..... $V^- - 0.3 < V_{IN} < V^+ + 0.3$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

Note 1.: This value of power dissipation refers to that of the package and will not normally be obtained under normal operating conditions.

TYPICAL OPERATING CHARACTERISTICS

$V^+ - V^- = 1.55V$, $f_{osc} = 32{,}768$ Hz, circuit in Figure 1, $T_A = 25°C$, unless otherwise stated.
Numbers are in absolute values.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	I^+	No Load		0.4	0.8	μA
Operating Voltage	$V^+ - V^-$	$0°C < T_A < 50°C$	1.2		1.8	V
Oscillator Transconductance	g_m	Start-up	15			μmho
Oscillator Capacitance	C_{OSC}		16	20	24	pF
STOP Input Current	I_{STOP}				0.3	μA
TEST Input Current	I_{TEST}				10	μA
Oscillator Stability	f_{STAB}	$\Delta(V^+ - V^-) = 0.6V$		0.1		ppm
Supply Current During Stop	I^+	'STOP' Connected to V^+			1.0	μA
Output Saturation Resistance	R_O	Bipolar (N-CH. + P-CH) $I_L = 1$ mA			200	Ω
Output Saturation Resistance P-CH	R_{O-P}	Unipolar $I_L = 3$ mA			200	Ω
Output Saturation Resistance N-CH	R_{O-N}	Unipolar $I_L = 3$ mA			50	Ω

7

TYPICAL WATCH CIRCUIT

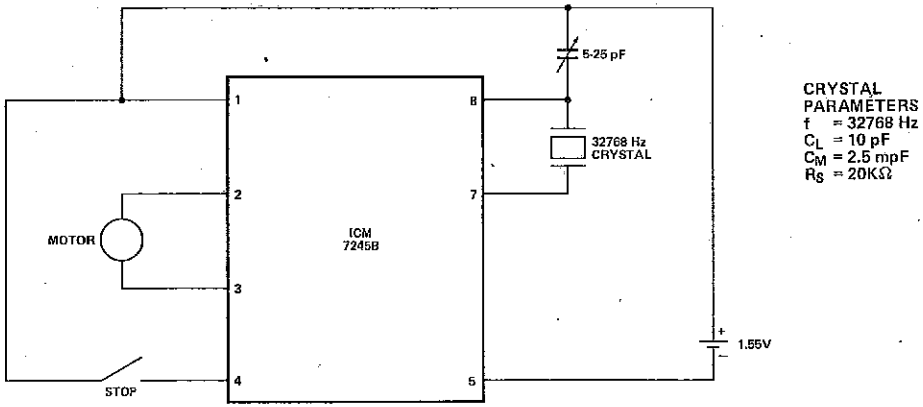
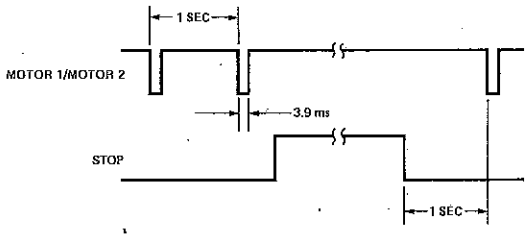


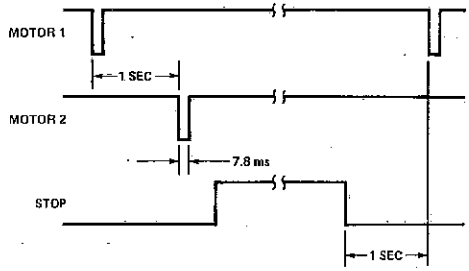
Figure 1.

WAVEFORMS

(ICM7245U)

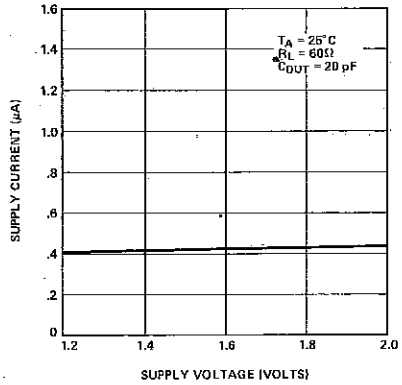


(ICM7245B)

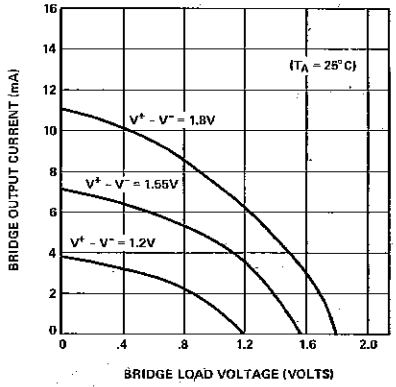


TYPICAL OPERATING CHARACTERISTICS

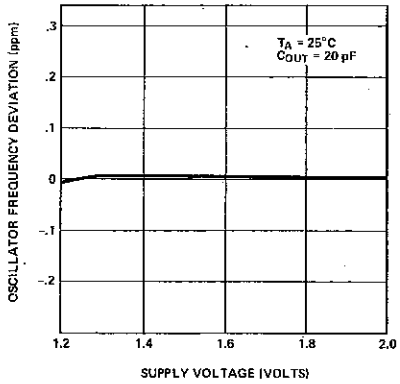
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



BRIDGE OUTPUT CURRENT AS A FUNCTION OF LOAD VOLTAGE



OSCILLATOR STABILITY AS A FUNCTION OF SUPPLY VOLTAGE



APPLICATION NOTES

OSCILLATOR

The oscillator of the ICM7245 is designed for low frequency operation at very low current from a 1.55 volt supply. The oscillator is of the inverter type, using a non-linear feedback resistor having maximum resistance under start-up conditions. The nominal load capacitance of the crystal should be less than 12 pF, with a preferred range of 7-10 pF. In specifying the crystal, the motional capacitance, series resistance and tuning tolerance must be compatible with the characteristics of the circuit to insure start-up and operation over a wide voltage range under worst case conditions.

The following expressions can be used to arrive at a crystal specification:

Tuning Range

$$\frac{\Delta f}{f} = \frac{C_m}{2(C_O + C_L)} \; ; \; C_L = \frac{C_{IN}\, C_{OUT}}{C_{IN} + C_{OUT}}$$

g_m required for start-up

$$g_m = 4\pi^2 f^2 C_{IN}\, C_{OUT}\, R_S \left(1 + \frac{C_O}{C_L}\right)^2$$

where

R_S = Series Resistance of Crystal
f = Frequency of the Crystal
Δf = Frequency Shift from Series Resonance Frequency
C_O = Static Capacitance of Crystal
C_{IN} = Input Capacitance
C_{OUT} = Output Capacitance
C_L = Load Capacitance
C_m = Motional Capacitance of Crystal

The g_m required for start-up calculated should not exceed 50% of the g_m guaranteed for the device.

TEST POINT

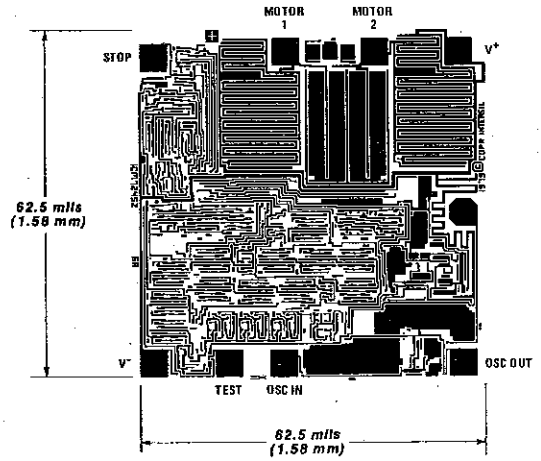
The TEST input, when connected to V^-, causes the ICM7245B/U to speed-up the outputs by 16 times. On long period output versions (12, 20, 60 sec) the speed-up factor will be larger. This allows easy testing of the finished watch module. The pulse width is not affected by the speed-up of the pulse frequency.

CUSTOM VERSIONS

The ICM7245 may be modified with alternative metal masks to provide different number of dividers, various pulse widths, and different output configurations.

In addition, MOS capacitors on-chip up to a total of 50 pF may be connected to either the input and/or the output of the oscillator. Consult your Intersil representative or the factory for further information.

CHIP TOPOGRAPHY

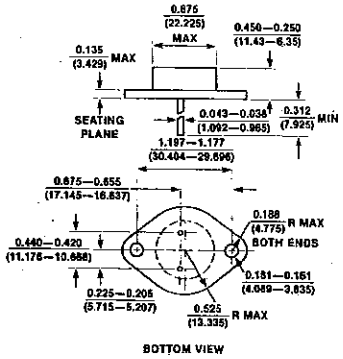


DIE SIZE = 62.5 x 62.5 MILS (1.58 x 1.58 mm)
BOND PAD SIZE = 5x5 MILS (.127 x .127 mm)

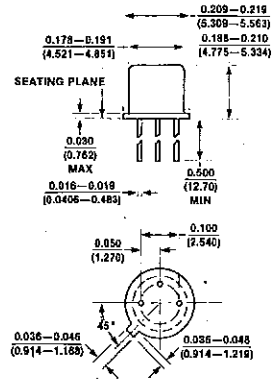
Appendix

PACKAGE OUTLINES

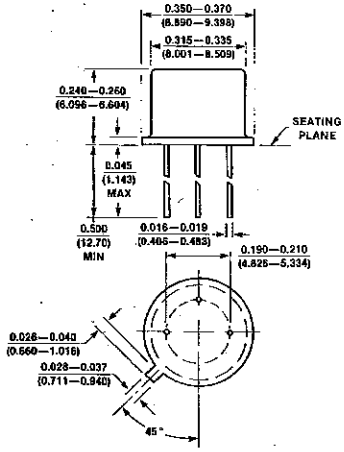
All dimensions given in inches and (millimeters).



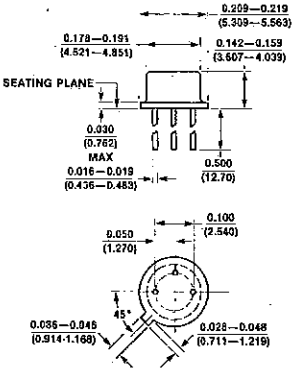
TO-3



TO-18

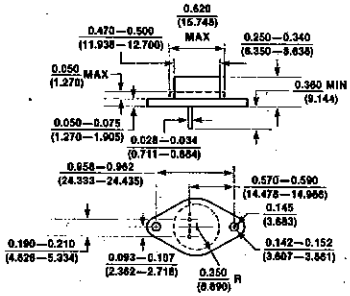


TO-39

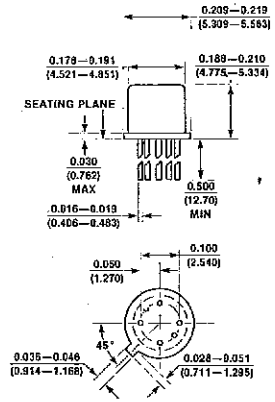


TO-52 (SQ*, SR)

*SQ denotes a two lead package; center lead missing.

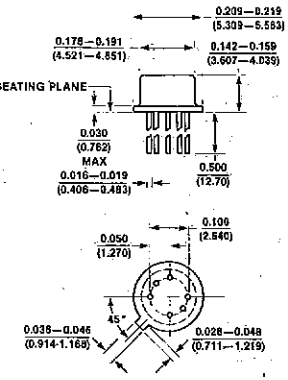


TO-66

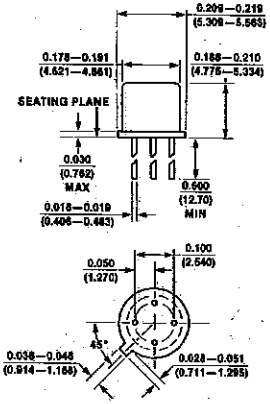


TO-71

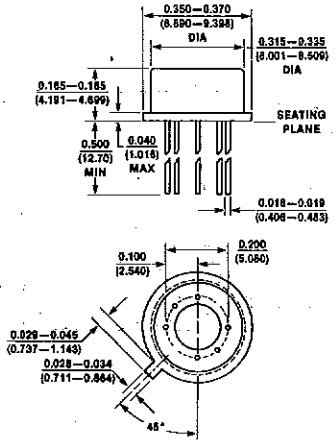
PACKAGE OUTLINES All dimensions given in inches and (millimeters).



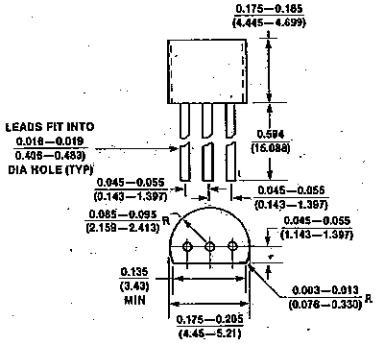
TO-71 LOW PROFILE (UT)



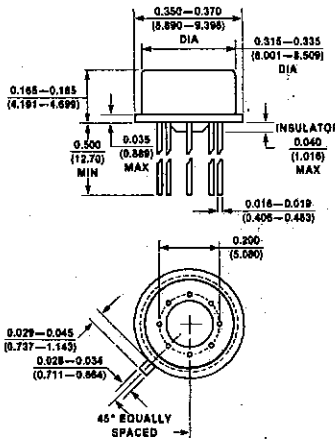
TO-72 (US)



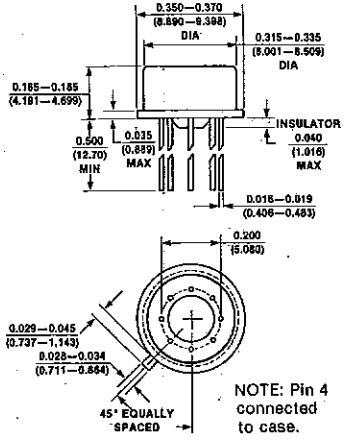
TO-78



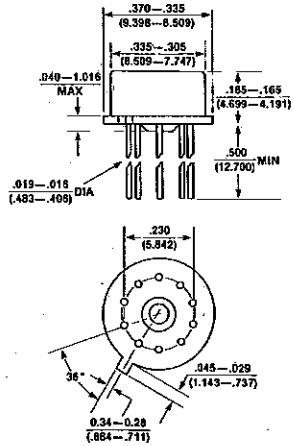
TO-92 (ZR)



TO-99 (TV)



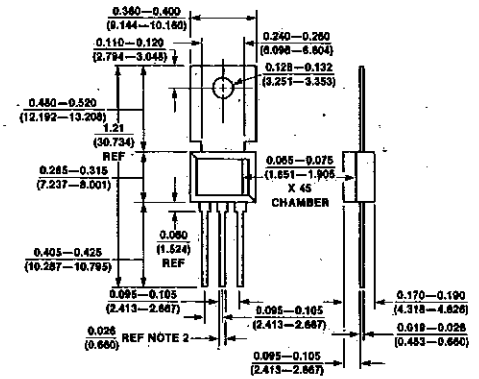
TO-99 (TY)



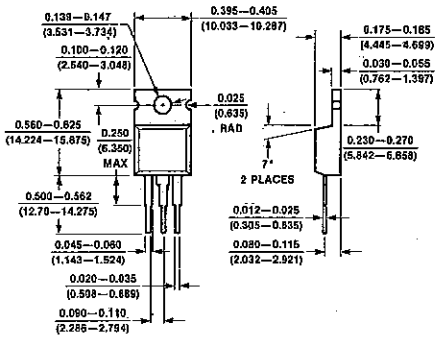
TO-100 (TW, TX)

B

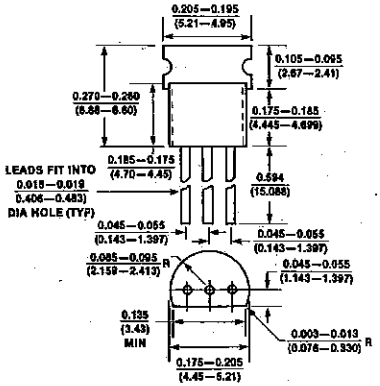
PACKAGE OUTLINES All dimensions given in inches and (millimeters).



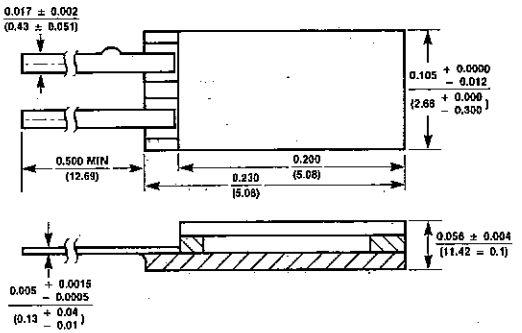
TO-202



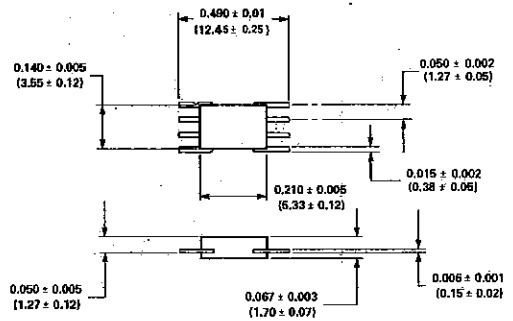
TO-220



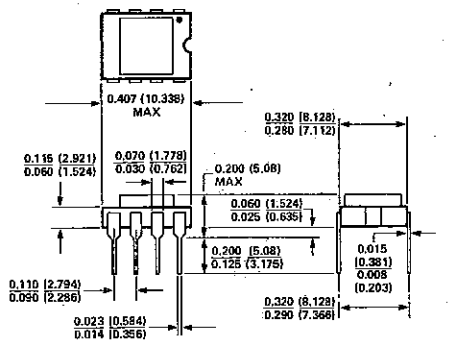
TO-237 (AR)



2 LEAD CERAMIC (DH)



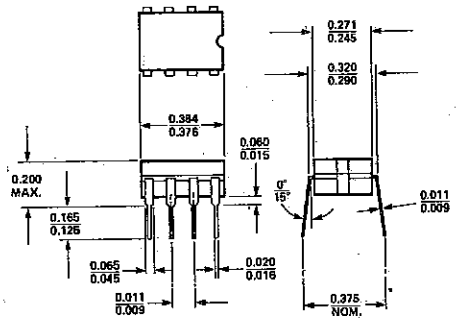
8 LEAD FLATPACK (BA)



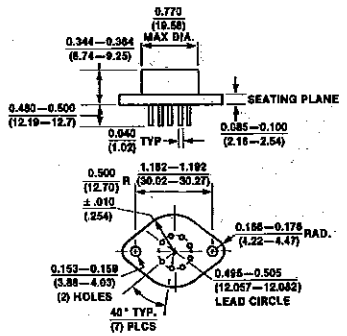
8 LEAD CERAMIC (DA)

B

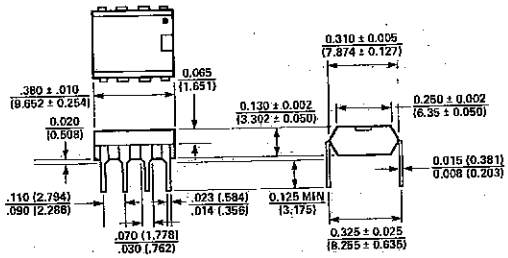
PACKAGE OUTLINES All dimensions given in inches and (millimeters).



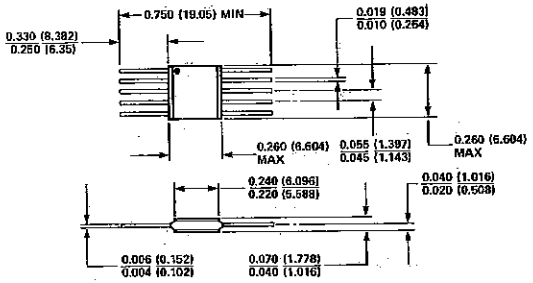
8 LEAD CERDIP (JA)



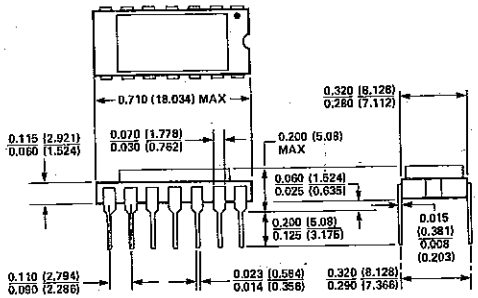
8 LEAD TO-3 CAN (KA)



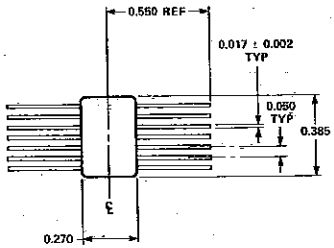
8 LEAD PLASTIC (PA)



10 LEAD FLATPACK (FB)

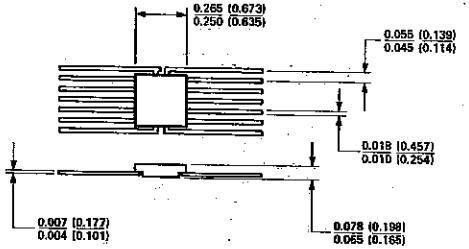


14 LEAD CERAMIC (DD)

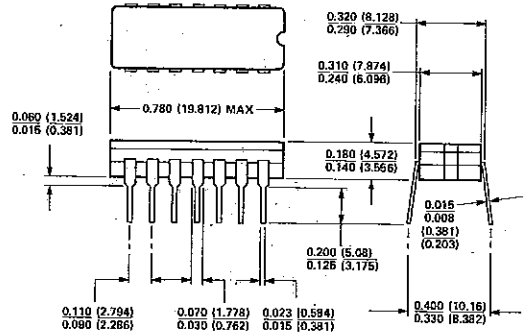


14 LEAD FLATPACK (FD-1)

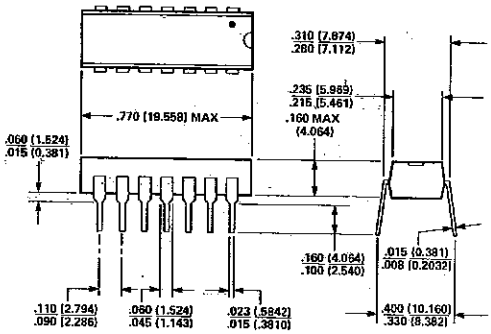
PACKAGE OUTLINES All dimensions given in inches and (millimeters).



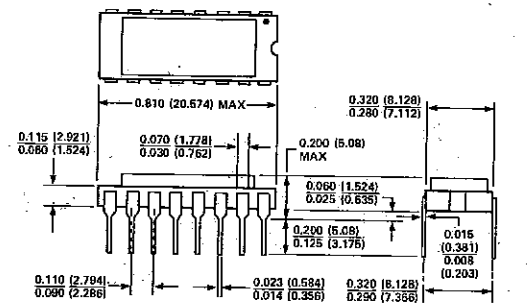
14 LEAD FLATPACK (FD-2)



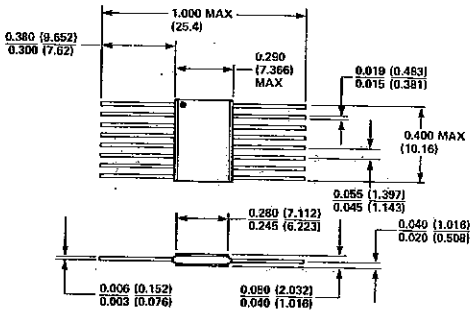
14 LEAD CERDIP (JD)



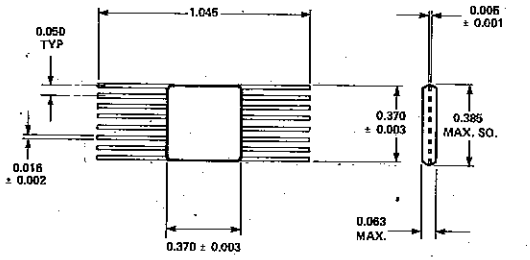
14 LEAD PLASTIC (PD)



16 LEAD CERAMIC (DE)

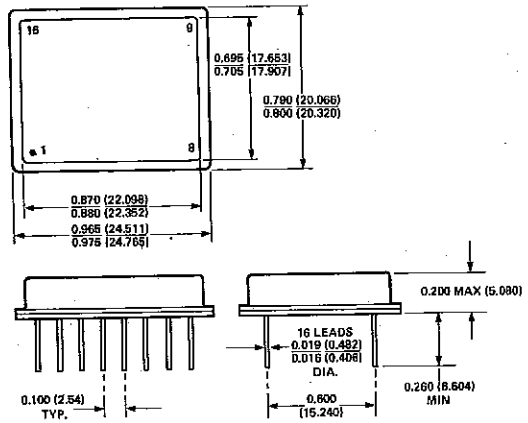


16 LEAD FLATPACK (FE-1)

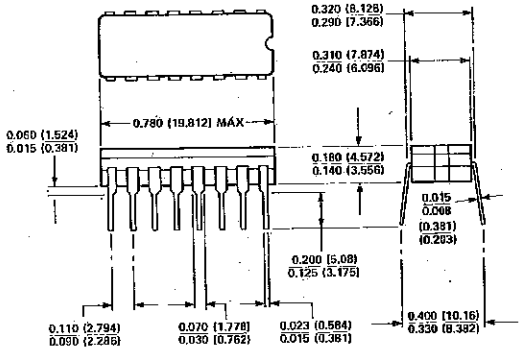


16 LEAD FLATPACK (FE-2)

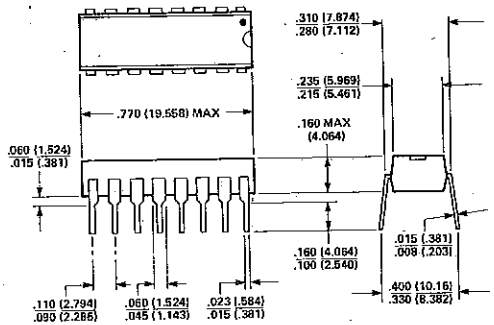
PACKAGE OUTLINES All dimensions given in inches and (millimeters).



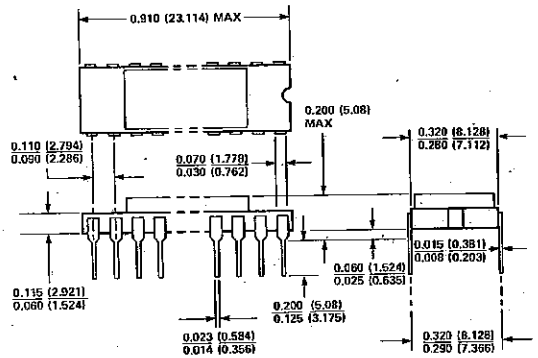
16 LEAD (.6 x .7) CERAMIC (IE)



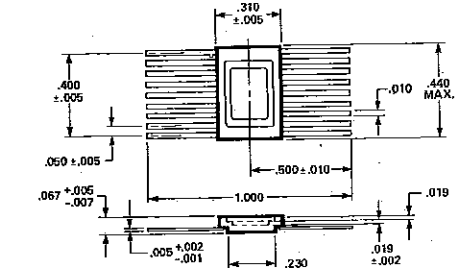
16 LEAD CERDIP (JE)



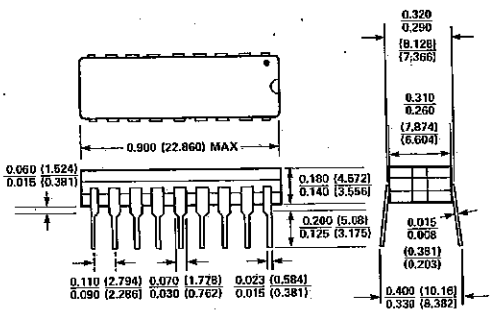
16 LEAD PLASTIC (PE)



18 LEAD CERAMIC (DN)

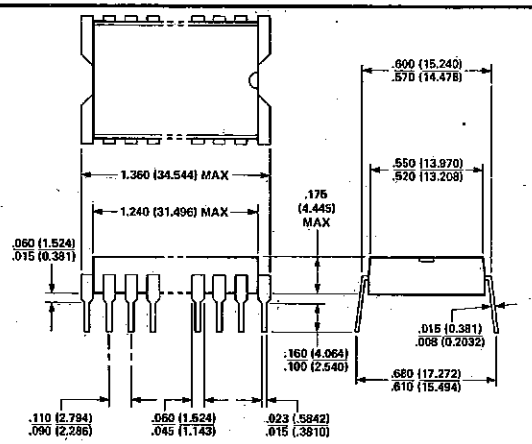


18 LEAD FLATPACK (FN)

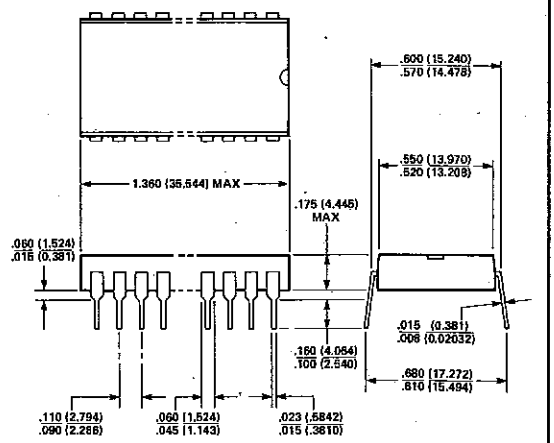


18 LEAD CERDIP (JN)

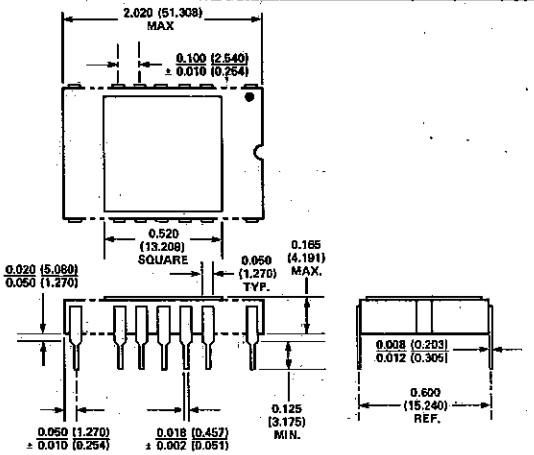
PACKAGE OUTLINES All dimensions given in inches and (millimeters).



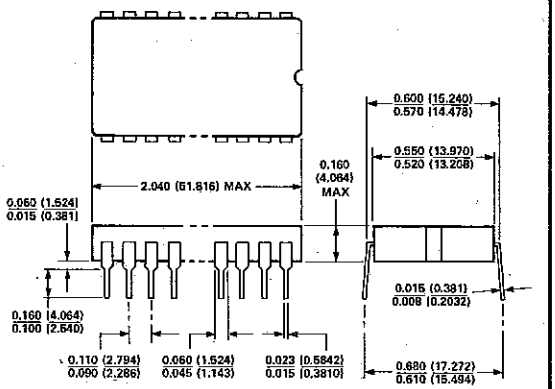
28 LEAD PLASTIC (PI-1)



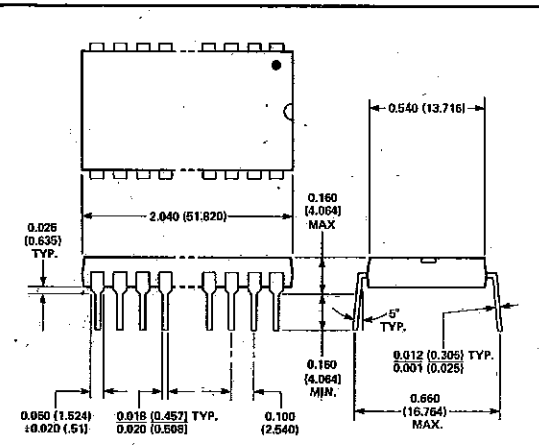
28 LEAD PLASTIC (PI-2)



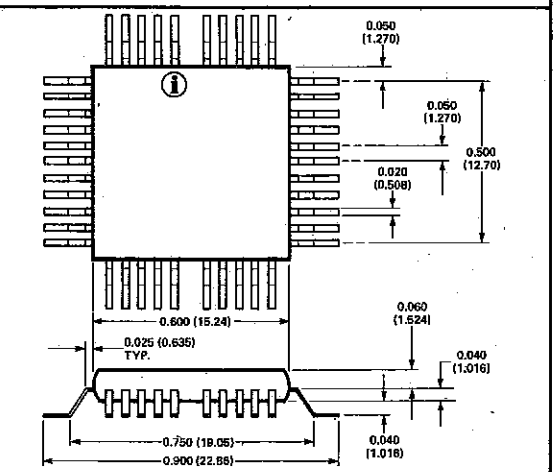
40 LEAD CERAMIC (DL)



40 LEAD CERDIP (JL)



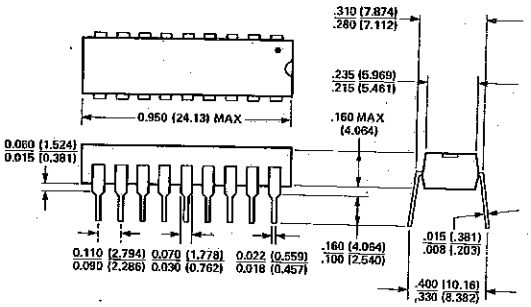
40 LEAD PLASTIC (PL)



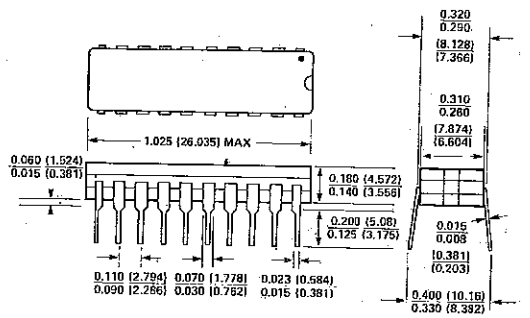
42 PIN FLATPACK (BH)

B

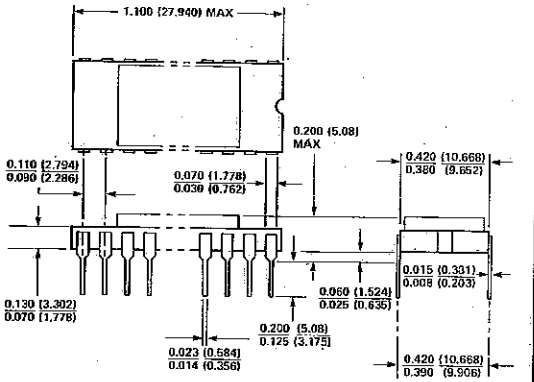
PACKAGE OUTLINES All dimensions given in inches and (millimeters).



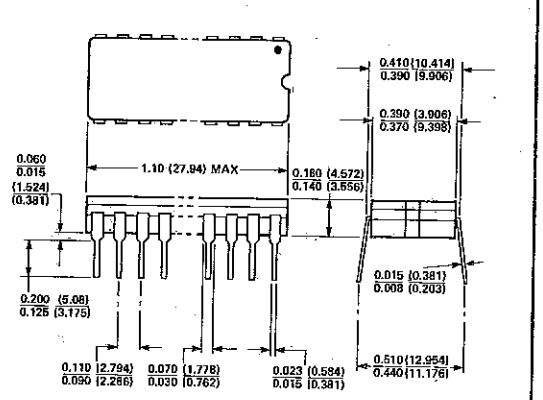
18 LEAD PLASTIC (PN)



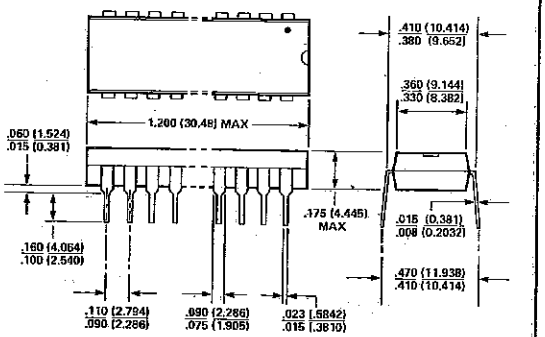
20 LEAD CERDIP (JP)



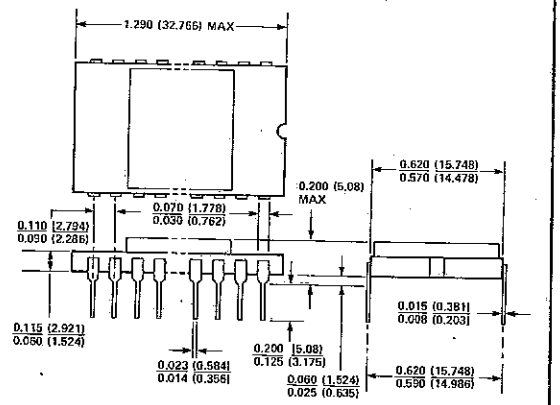
22 LEAD CERAMIC (DF)



22 LEAD CERDIP (JF)

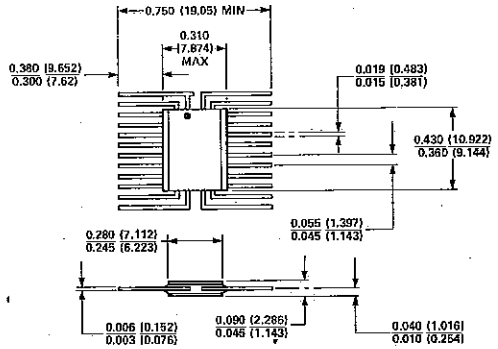


22 LEAD PLASTIC (PF)

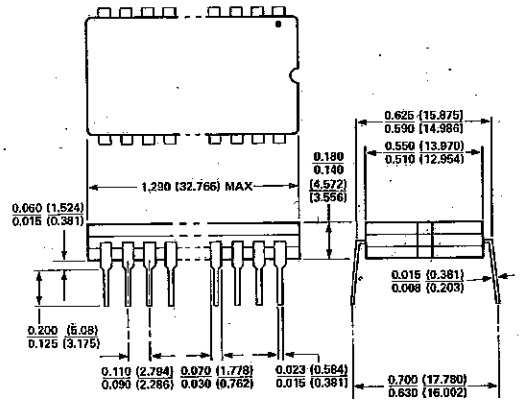


24 LEAD CERAMIC (DG)

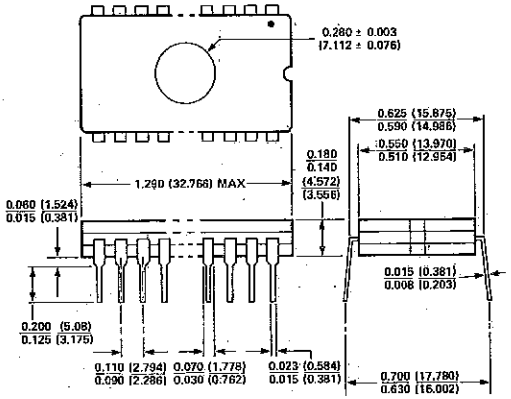
PACKAGE OUTLINES All dimensions given in inches and (millimeters).



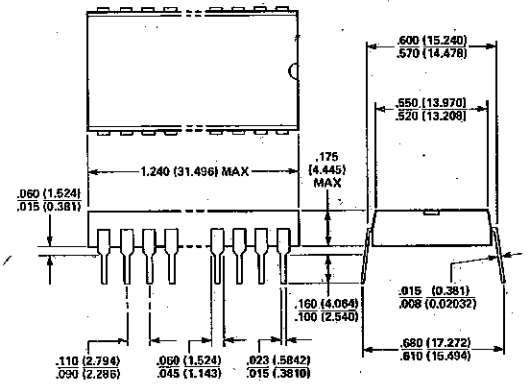
24 LEAD FLATPACK (FG)



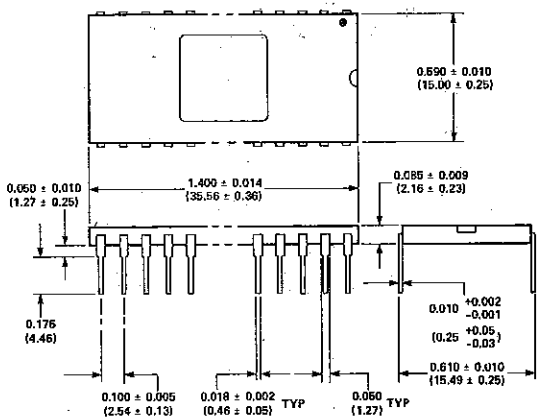
24 LEAD CERDIP (JG)



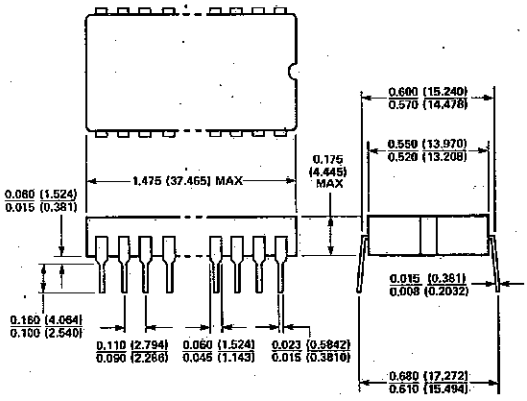
24 LEAD CERDIP WITH WINDOW (JG/W)



24 LEAD PLASTIC (PG)



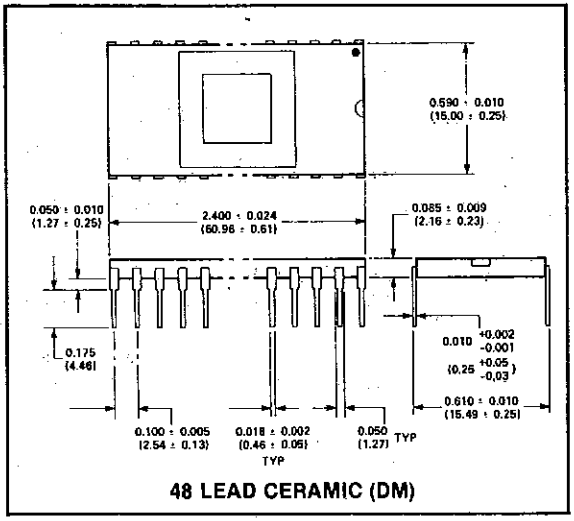
28 LEAD CERAMIC (DI)



28 LEAD CERDIP (JI)

B

PACKAGE OUTLINES All dimensions given in inches and (millimeters).



48 LEAD CERAMIC (DM)

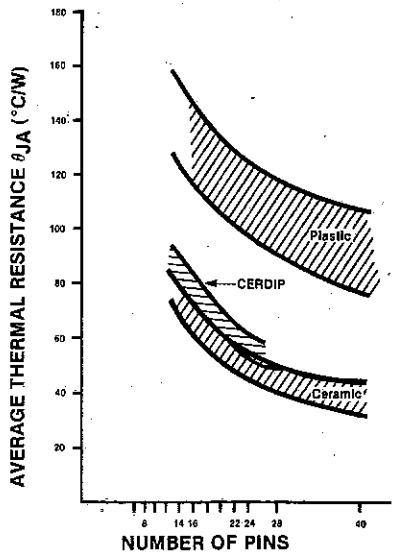
THERMAL RESISTANCE θ_{JA}

The junction-to-ambient thermal resistance values of dual in-line packaging systems used in GE Intersil CMOS integrated circuits are graphically illustrated in Figure 1. Each envelope represents the typical range of values for plastic, CERDIP or ceramic sidebraze package types as a function of size. The values were obtained while operating in a "still-air" environment and inserted into low-cost sockets mounted on printed circuit cards.

Thermal resistance is influenced by a number of factors including die size, cavity size and die bonding. In order to present a comprehensive characterization of these variables, a range of values is provided rather than a single point.

Since most CMOS devices dissipate insignificant power, it is not likely that thermal resistance will be a critical design factor. In those situations where high dc currents or high-speed operation is required, the junction temperatures should be estimated through the use of this data and by knowing the actual power being dissipated by the device.

Figure 1 — THERMAL RESISTANCE OF DIP PACKAGES



B

100% INTEGRATED CIRCUIT PROCESSING

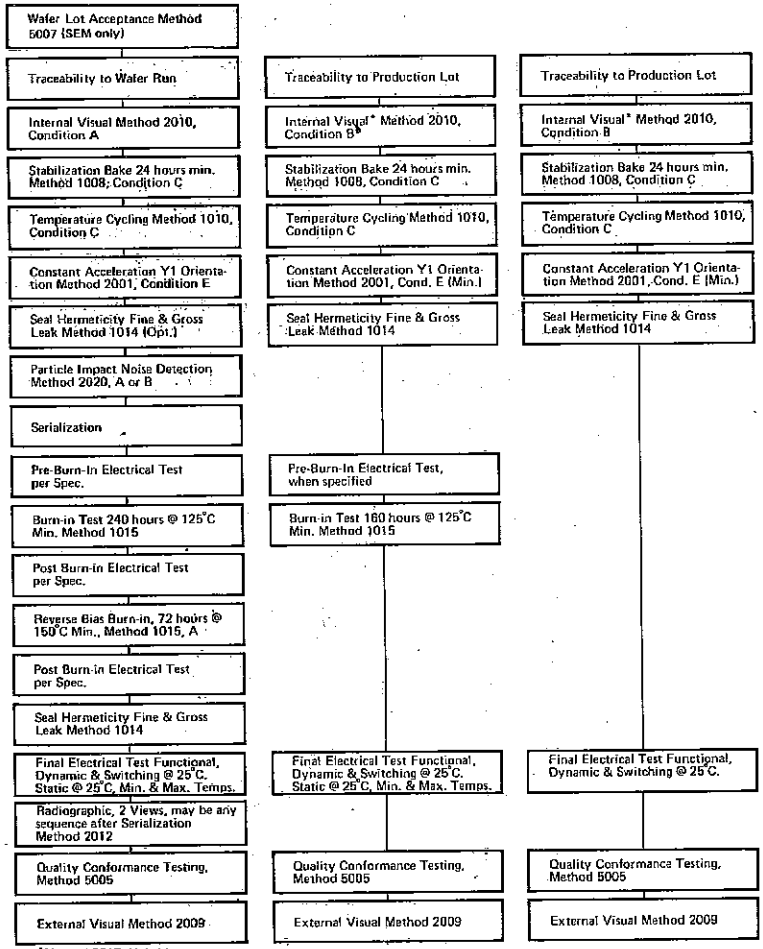
Intersil is committed to build and process integrated circuits for the Military/High-Rel market segments in conformance with MIL-STD-883 and MIL-M-38510. Any customer drawing which specifies testing as set forth in these documents will be automatically processed to the latest revisions of MIL-STD-883 and MIL-M-38510, unless specific requests are made to the contrary.

100% DISCRETE DEVICE PROCESSING

Intersil also offers several QPL-approved discrete products carrying the JANTX designation, which are screened and qualified to the latest revisions of MIL-STD-750 and MIL-S-19500.

MIL-STD-883B SCREENING AND QUALITY CONFORMANCE PROGRAMS, METHODS 5004 AND 5005

The following flow chart details screening activities as carried out by Intersil for Class S, B and C requirements.

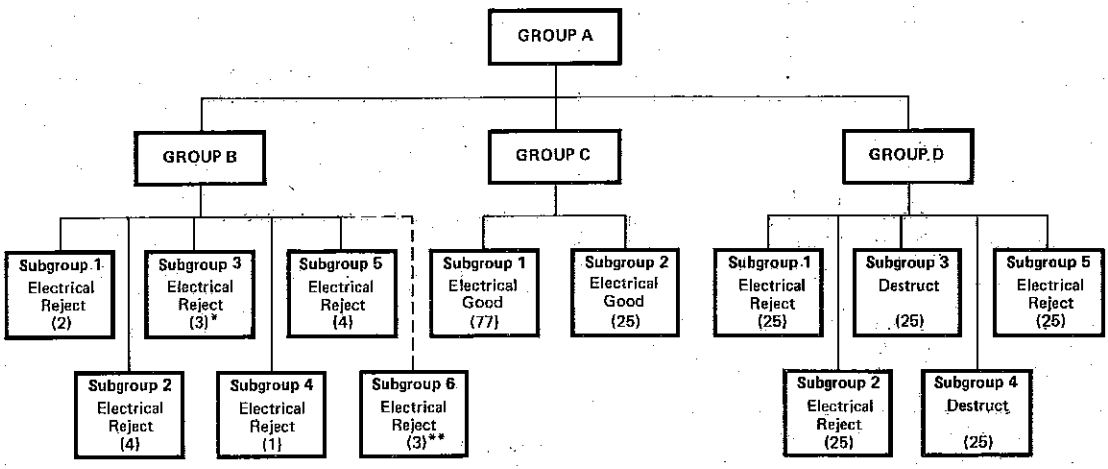


*Method 2017, Hybrid

B

QUALITY CONFORMANCE INSPECTION, CLASSES B AND C

The following diagram presents quality conformance inspection methods for Classes B and C as performed at Intersil.



*Sample must have had temp/time exposure specified for burn-in. LTPD of 15 applies to number of leads inspected except that in no case shall less than 3 devices be used.

**Required only when a package contains a dessicant.

NOTES:

1. Group A and B inspections are required on individual inspection lots as a condition for acceptance for delivery.
2. Samples shall be randomly selected from the assembled inspection lot in accordance with appendix B of MIL-M-38510. Specified screen requirements of method 5004 are not required to have been completed for Intersil's standard generic data program, but will be performed when required by customer drawing. Where use of electrical rejects is permitted, and unless otherwise specified, they need not have been subjected to the temperature/time exposure of burn-in.
3. Group C (chip-related test) shall be performed periodically at 3 month intervals.
4. Group D (package related tests) shall be performed periodically at 6 month intervals.
5. Where end point measurements are required but no parameters have been identified, the critical final electrical parameters specified for 100% screening shall be used as end point measurements.
6. Subgroups within a group may be performed in any order but individual tests within a subgroup shall be performed in the sequence indicated.

QUALITY CONFORMANCE

The following steps are carried out when quality conformance testing is performed on a lot from which samples are taken.

QUALITY CONFORMANCE – CLASSES B & C

	STANDARD SAMPLE SIZE	ALLOWABLE REJECTS	TIME ALLOWANCE
Group A (Electrical Acceptance)	45	0	3–5 days
Group B (Package Related)	14 Electrical Rejects	0	1 week
Group C (Die Related)	102 Good Electrical (Note 1)	1 from Subgroup 1 1 from Subgroup 2	8–10 weeks
Group D (Package Related)	50 Good Electrical (Note 2) 75 Electrical Rejects	1 from each of 5 Subgroups	4 weeks

NOTE 1: Non-destructive, shippable samples (102 units).

NOTE 2: Destructive tests:

Moisture resistance. Subgroup 3 sample size	25 units
Variable-frequency vibration. Subgroup 4 sample size	25 units
Total Destroyed	50 units

QUALIFICATION TESTING

When qualification testing is required, it will be equivalent to quality conformance testing, with the exception that Group A must be read and recorded on all applicable subgroups for the number of electrically-good units which will be required for samples for Groups C and D.

QUALIFICATION TESTING – GROUPS B & C

	STANDARD SAMPLE SIZE	ALLOWABLE REJECTS	TIME ALLOWANCE
Group A (Electrical Acceptance)	184 (Read & Record)	5	5 days
Group B (Package Related)	14 Electrical Rejects	0	1 week
Group C (Die Related)	102 Good Electrical (Note 1)	1 from Subgroup 1 1 from Subgroup 2	10–12 weeks
Group D (Package Related)	50 Good Electrical (Note 2) 75 Electrical Rejects	1 from each of 5 Subgroups	4 weeks

NOTE 1: Shippable samples.

LIMITED USAGE QUALIFICATION

A customer may elect to take advantage of a "Limited Usage" qualification per MIL-M-38510, in order to reduce the number of samples required. The following conditions must be met for eligibility for the "Limited Usage" qualification:

1. A maximum quantity of 500 microcircuits is included in a single order.
2. A maximum quantity of 2000 microcircuits is included in a given equipment-acquisition contract or program.
3. A maximum quantity of 2000 microcircuits is to be procured during a 12-month period for a given circuit type and vendor.

Microcircuits which qualify for limited usage cannot be assigned a JAN part number. Variable data will be taken only when specified in a customer drawing.

LIMITED USAGE QUALIFICATION – CLASS B[1]

	SAMPLE SIZE	ALLOWABLE REJECTS	TIME ALLOWANCE
Group A (Electrical Acceptance)	45	0	5 days
Group B (Package Related)	14 Electrical Rejects	0	1 week
Group C (Die Related, Non-Destructive)	10 Good Electrical Parts	0	8–10 weeks
Group D (Package Related, Destructive)	25 (15 Good, 10 Electrical Rejects)	0	4 weeks

(1) Mil-M-38510, Paragraph 4.4.4; MIL-STD-883, Method 5005.

B

GLOSSARY OF MILITARY/AEROSPACE HIGH-REL DEFINITIONS/TERMINOLOGY

ACCELERATED BURN-IN – Same as "Burn-In", except that testing is carried out at an increased temperature (nominally 150° C) for reduced dwell time. Accelerated testing is not permissible for Class S devices.

ATTRIBUTES DATA – Go-No-Go data. Strictly pass/fail and number of rejects recorded. A typical requirement for post burn-in electrical tests on Class B devices.

BASELINE – Technique used to define manufacturing and test processes at time of order placement. Baselining usually involves development of a Program Plan and an Acceptance Test Plan which include flow charts, specification identification/revision letters, QA procedures, and actual specimens of certain important specifications. During subsequent manufacture and testing of parts, it is not permissible to make revisions or changes to any of the identified specifications, unless prior notification and possible customer approval occurs. Other terminology associated with baselining include "Critical Process Changes", "Minor Process Changes", and "Major Process Changes".

BURN-IN – A screening operation. Devices are subjected to high temperature (typically 125° C) and normal power/operation for 160 hours (Class B devices) or 240 hours (Class S devices).

CLASS S, B AND C INTEGRATED CIRCUITS – These classes set forth the screening, sampling and document control requirements for IC testing. Terminology is defined in MIL-M-38510 and in Test Methods 5004 and 5005 of MIL-M-38510. Classes, S, B and C are sometimes referred to as "Levels S, B and C." The Classes cover:

CLASS S – For space and satellite programs. Includes Condition A Precap, SEM, 240 hour burn-in, PIND test and elaborate qualification and quality conformance testing. Normally requires extensive data, documentation, and program planning. Formerly referred to as Class A. Class S devices are quite expensive.

CLASS B – For manned flight, and includes most frequently-procured military integrated circuits. Used for all but highest reliability requirements. Class B uses burn-in, pre-cap visual, etc.

CLASS C – For ground support equipment. Contains only environmental screening requirements with pre-cap visual. No burn-in required.

In all classes, LTPD (Lot Tolerance Percent Defective) is the sampling plan measurement criteria.

CORRECTIVE ACTION – Those actions which a given supplier (or user) agrees to perform so that a detected prob-

DESC – Defense Electronic Supply Center, located in Dayton, Ohio. The command includes two major subgroups, with functions as follows:

DESC-ECS – This group performs specification engineering work. After the original specifications are created at RADC, DESC-ECS implements and monitors the specifications. DESC-ECS is the industry's main interface on existing specifications.

DESC-EQM – The group which supervises supplier certifications and qualifications per MIL-M-38510. The group to which the industry submits applications when desiring to have devices qualified (QPL'd) on an existing JAN slash sheet. DESC-EQM surveys supplier facilities and grants line certification as various requirements are met. Also reviews manufacturer's qualification test data and issues JAN QPL's accordingly.

DESC-EQT – Same as EQM, except handles transistors per MIL-S-19500.

DESC LINE CERTIFICATION – The document which approves a supplier's facilities as an appropriate site to manufacture JAN parts.

DIE SHEAR TESTS – A sample test. Mounted chips are exercised to destruction. Degree of die adherence to lead frame is observed. Corrective action taken if required.

DPA – Destructive Physical Analysis. Finished products are opened and analyzed, in accordance with customer or MIL Spec criteria.

GENERIC DATA – Data pertaining to a device family; not necessarily the specific part number ordered by the customer, but representative of parts in the family. Group B, C and D generic data is frequently requested in lieu of the performance of special qual tests on a given order.

GROUP A – Sample electrical tests which are performed on each lot. Group A is defined in Test Method 5005 for integrated circuits and in MIL-S-19500 for diodes and transistors.

GROUP B – A collection of package-related environmental and "wear-and-tear" tests. Defined in Test Method 5005 for integrated circuits. For Class S screening, additional life tests are required, and are performed on every lot per MIL-M-38510. For diodes and transistors, Group B consists of both environmental and life tests, as defined in MIL-S-19500.

GROUP C – For Class B and C integrated circuits, only Group C includes life testing and temperature cycling/constant acceleration die-related sample tests. Defined in Test Method 5005 and performed every three months per MIL-M-38510.

GROUP D – A collection of additional environmental package-related sample tests as defined in Test Method 5005. Performed every six months per MIL-M-38510. For classes S, B, & C.

JAN — "Joint Army Navy", a registered trademark of the U.S. Government. The JAN marking denotes a device which is in full compliance to MIL-M-38510 or MIL-S-19500.

JAN TX — A JAN-qualified diode or transistor which has been subjected to additional screening (burn-in) tests. MIL-S-19500 only.

JAN TXV — A JAN-qualified diode or transistor which, in additional to burn-in testing, has been subjected to additional screening including pre-cap visual inspection, as witnessed by a government source inspector. Equivalent to Class B screening for integrated circuits. MIL-S-19500 only.

"M38510" CIRCUITS — Until a recent revision to MIL-M-38510, it was a common practice for users and suppliers alike to specify or offer integrated circuits marked "M38510/XXX" without a J or JAN prefix. This part numbering system indicated a device which was "near-JAN", "quasi-JAN" or "non-JAN". The practice tended to cause confusion between these devices and parts in full conformance to JAN levels. MIL-M-38510 now prohibits such marking with the exception of two special instances:

- When JAN QPL supplier for a given product does not exist, the government will permit "M38510/XXX" marking. While a customer may specify such marking, the supplier must furnish the government with evidence that the parts meet all applicable requirements.
- For certain parts destined for use in some programs, "M38510/XXX" marking is permissible, but orders for such parts must be accompanied by appropriate DESC certification letter.

M38510/XXX — Detail specifications (or "slash sheets") for integrated circuits. For example, the 101 specification covers Operational Amplifiers, with electrical requirements for the 741, LM101, 108, 747 types, etc.

MIL-M-38510 — The general military specification for integrated circuits.

MIL-S-19500 — The general military specifications for diodes and transistors.

MIL-S-19500/XXX — Detail specifications (or "slash sheets" for diodes and transistors.

MIL-STD-750 — Specifies Test Methods for diodes and transistors, such as burn-in, pre-cap, temperature cycling, etc.

MIL-STD-883 — Specifies Test Methods for integrated circuits, such as pre-cap, burn-in, , hermeticity, storage life, etc.

NPFC — Naval Publications and Forms Center, Philadelphia. Printing and distribution source for military specifications.

NON-STANDARD PARTS — In government terminology, refers to non-JAN devices. Non-standard parts are typically covered by user Source Control Drawings (SCD).

NON-STANDARD PARTS APPROVAL — Approval by the government (frequently RADC) of non-JAN parts, typically on source control drawings, for use in a military system or program. This approval is essentially a waiver which permits non-JAN 38510 parts in a system which otherwise mandatorially requires JAN parts only.

OPERATING LIFE TEST — Same conditions as burn-in, but duration is usually 1000 hours. This is a sample test (Qualification and Quality Conformance).

PCA — Parts Configuration Analysis. A new term which has much the same meaning as "Baseline".

PDA — Percent Defective Allowable. Criteria sometimes applied to burn-in screening. A 10% PDA (the most common type) means that if more than 10% of that lot fails as a result of burn-in (as determined by pre- and post-burn-in electrical tests) the entire lot is considered to have failed.

PDS — Parameter Drift Screening. Measures the changes (Δs) in electrical parameters through burn-in. Common for Class S devices.

PIND — Particle Impact Noise Detection. This is an audio screening test to locate and elminate those parts which have loose internal particles. The test can isolate a high percentage of defectives, even in otherwise good lots. Repeatability of the tests is questionable. This test is one of the screening items for Class S integrated circuits.

PREPARING ACTIVITY — The organizational element of the government which writes specifications, frequently RADC.

PRESEAL VISUAL — A screening inspection which involves observation of a die through a microscope.

PROCURING ACTIVITY — Per MIL-M-38510, this is the organizational element in the government which contracts for articles or services. The Procuring Activity can be a subcontractor (OEM), providing that the government delegates this responsibility. In such a case, the subcontractor does not have the power to grant waivers, unless this authority has been approved by the government.

PRODUCT RELIABLIITY — Pertains to the level of quality of a product over a period of time. Reliability is usually measured or expressed in terms of Failure Rate (such as "0.002% per 1000 hours at a 60% confidence level at 25°C") or MTBF (mean time between fallure in hours). MTBF is the reciprocal of Failure Rate.

QPL — Qualified Products List. In the case of JAN products, QPLs are identified as QPL-38510 for integrated circuits and QPL-19500 for diodes and transistors. QPL-38510 revisions occur approximately quarterly and QPL-19500 revisions occur approximately annually. In the interim, the government will notify suppliers via letter of any new device qualifications which may have been granted. Two types of QPLs exist for MIL-M-38510:

PART II QPL — This is an interim or temporary QPL which is granted on the basis of having obtained line certification and approval of an Application to Conduct Qualification Testing. A PART II QPL is automatically voided after 90 days whenever any one supplier is granted a PART I QPL.

PART I QPL — A "permanent" QPL, granted after all qualification testing is completed and test data is approved by the government.

QPLTT — Qualified Product List Throughput Time. That period which required to obtain device qualification. QPLTT is a function of (1) whether a JAN slash sheet exists; (2) whether a competitor already holds a Part I QPL; and (3) whether the applicant's production line is certified by DESC.

Following is a worst-case example, where a JAN slash sheet does not exist and government line certification has not been granted. QPLTT will be approximately 39.5 months, if the JAN slash sheet already exists, QPLTT will be cut to about 10.5 months. If the applicant already has line certification, QPLTT will be about 2 months to obtain Part II status.

Total time required to obtain a Part I QPL adds about 7 months to QPLTT; in a worst-case example, about 46 months will be required.

QUALIFYING ACTIVITY — Per MIL-M-38510, the organizational element in the government which designates certification (i.e., DESC).

QUALIFICATION TESTING — Initial one-time sample tests which are performed to determine whether device types and processes are good. For integrated circuits, this usually means testing to Groups A, B, C and D. For diodes and transistors, this usually means testing to Groups A, B and C.

QUALITY CONFORMANCE TESTING — These are sample tests which must be performed at prescribed intervals per MIL-M-38510 or MIL-S-19500, assuring that processes remain in control and that individual lots are passed.

RADC — Rome Air Development Command, Griffiss AFB, New York. This is the government organization which created semiconductor specifications; MIL-M-38510 and MIL-STD-883 were developed at RADC. This Air Force unit develops specifications for all U.S. military services. RADC is frequently involved in granting waivers for non-standard parts for Air Force systems.

READ AND RECORD DATA — Same as variable data.

REWORK PROVISION — For semiconductor devices, permissible rework of parts is usually limited to re-testing (screening), lead straightening or bending, re-marking, and cleaning.

S & V — Survivability and Vulnerability. Pertains to the

SCREENING — Operations which are performed on devices on a 100% basis (not sampling). Examples include pre-cap visual, burn-in hermeticity, 100% electrical test, etc. For integrated circuits, Test Method 5004 defines screening flow.

SEM INSPECTION — Inspection by Scanning Electron Microscope. Die samples are examined at very high magnification for metallization defects. A common inspection for Class S devices.

SERIALIZATION — The marking of a unique part number on each part, with assigned numbers marked sequentially/consecutively.

SCDs — Source Control Drawings. Typically user-generated drawings which require development of internal IC vendor sheets. Although each drawing may be slightly different, all will be modelled around MIL-M-38510, MIL-S-19500, MIL-STD-883, or MIL-STD-750.

SOURCE INSPECTION — Can be either Customer Source Inspection (CSI) or Government Source Inspection (GSI). Source Inspection is initiated via purchase order, and can occur at one or more of the following points:

- Pre-cap Visual. Expensive and adds to throughput time.
- Final Inspection. Simple and inexpensive; little delivery impact.
- Throughout. Very expensive and time-consuming.

STANDARD PARTS — In government terminology, JAN parts.

TRACEABILITY — A production and manufacturing control system which includes:

- Wafer run identification number.
- Date pre-cap visual inspection was performed, identity of inspector, and specification number and revision.
- Lot number and inspection history.
- QA Group A electrical results.

VARIABLE DATA — Read and recorded electrical measurements (parametric values). Usually required for pre- and post-burn-in electrical tests. Also common for Group C and D testing.

WIRE PULL TESTS — Bond wire pull tests will be specified in two modes:

DESTRUCTIVE WIRE PULL — Generally performed periodically in assembly on a sample basis. Wires are pulled to destruction and the break point force is recorded. Corrective action is taken as required.

NON-DESTRUCTIVE WIRE PULL — Option for class B microcircuits, wire bonds are pulled to a max of 70% of the preseal minimum bond strengths for the applicable

Ordering Information for MIL-STD-883B Processed Devices

The following Intersil devices are available as a standard with Class B screening per method 5004 of MIL-STD-883B. To order, add 833B after the device number as shown below.

Part Number	Part Number	Part Number	Part Number
AD532SD/883B	DG112AL/883B	DG162AK/883B	DGM185AL/883B
AD532SH/883B	DG116AK/883B	DG162AL/883B	DGM187AA/883B
AD550M-12/883B	DG116AL/883B	DG163AK/883B	DGM187AK/883B
AD550S/883B	DG118AK/883B	DG163AL/883B	DGM187AL/883B
AD550T/883B	DG118AL/883B	DG164AK/883B	DGM188AA/883B
AD550U/883B	DG120AK/883B	DG164AL/883B	DGM188AK/883B
AD590JH/883B	DG120AL/883B	DG180AA/883B	DGM188AL/883B
AD590KH/883B	DG121AK/883B	DG180AK/883B	DGM190AK/883B
AD590LH/883B	DG123AK/883B	DG180AL/883B	DGM190AL/883B
AD590MH/883B	DG123AL/883B	DG181AA/883B	DGM191AK/883B
AD7520SD/883B	DG125AK/883B	DG181AK/883B	DGM191AL/883B
AD7520TD/883B	DG125AL/883B	DG181AL/883B	
AD7520UD/883B	DG126AK/883B	DG182AA/883B	G115AK/883B
AD7521SD/883B	DG126AL/883B	DG182AK/883B	G115AL/883B
AD7521TD/883B	DG129AK/883B	DG182AL/883B	G116AK/883B
AD7521UD/883B	DG129AL/883B	DG183AK/883B	G116AL/883B
AD7523SD/883B	DG133AK/883B	DG183AL/883B	G117AK/883B
AD7523TD/883B	DG133AL/883B	DG184AK/883B	G117AL/883B
AD7523UD/883B	DG134AK/883B	DG184AL/883B	G118AK/883B
AD7533SD/883B	DG134AL/883B	DG185AK/883B	G118AL/883B
AD7533TD/883B	DG139AK/883B	DG185AL/883B	G119AK/883B
AD7533UD/883B	DG139AL/883B	DG186AA/883B	G119AL/883B
AD7541SD/883B	DG140AK/883B	DG186AK/883B	G123AK/883B
AD7541TD/883B	DG140AL/883B	DG186AL/883B	G123AL/883B
ADC0801LD/883B	DG141AK/883B	DG187AA/883B	G125AK/883B
ADC0802LD/883B	DG141AL/883B	DG187AK/883B	G125AL/883B
ADC0803LD/883B	DG142AK/883B	DG187AL/883B	G126AK/883B
	DG142AL/883B	DG188AA/883B	G126AL/883B
D112AK/883B	DG143AK/883B	DG188AK/883B	G127AK/883B
D112AL/883B	DG143AL/883B	DG188AL/883B	G127AL/883B
D113AK/883B	DG144AK/883B	DG189AK/883B	G128AK/883B
D113AL/883B	DG144AL/883B	DG189AL/883B	G128AL/883B
D120AK/883B	DG145AK/883B	DG190AK/883B	G129AK/883B
D120AL/883B	DG145AL/883B	DG190AL/883B	G129AL/883B
D121AK/883B	DG146AK/883B	DG191AK/883B	G130AK/883B
D121AL/883B	DG146AL/883B	DG191AL/883B	G130AL/883B
D123AK/883B	DG151AK/883B	DG200AA/883B	G131AK/883B
D123AL/883B	DG151AL/883B	DG200AK/883B	G131AL/883B
D125AK/883B	DG152AK/883B	DG200AL/883B	G132AK/883B
D125AL/883B	DG152AL/883B	DG201AK/883B	G132AL/883B
D129AK/883B	DG153AK/883B	DGM182AA/883B	
D129AL/883B	DG153AL/883B	DGM182AK/883B	ICL7109MDL/883B
	DG154AK/883B	DGM182AL/883B	ICL7650MJD/883B
DG111AK/883B	DG154AL/883B	DGM184AK/883B	ICL7650MTV/883B
DG111AL/883B	DG161AK/883B	DGM184AL/883B	ICL7660MTV/883B
DG112AK/883B	DG161AL/883B	DGM185AK/883B	ICL8007AMTV/883B

B

Part Number	Part Number	Part Number	Part Number
ICL8007MTY/883B	IH5009MJD/883B	IH5048MTW/883B	IM6402-1MJL/883B
ICL8013AMTZ/883B	IH5010MJD/883B	IH5049MFD/883B	IM6402AMJL/883B
ICL8013BMTZ/883B	IH5011MJE/883B	IH5049MJE/883B	IM6403-1MJL/883B
ICL8013CMTZ/883B	IH5012MJE/883B	IH5050MFD/883B	IM6403AMJL/883B
ICL8018AMJD/883B	IH5013MJD/883B	IH5050MJE/883B	
ICL8018MJD/883B	IH5014MJD/883B	IH5050MTW/883B	IM6512AMFN/883B
ICL8019AMJD/883B	IH5015MJE/883B	IH5051MFD/883B	IM6512AMJN/883B
ICL8019MJD/883B	IH5016MJE/883B	IH5051MJE/883B	IM6512MFN/883B
ICL8020AMJD/883B	IH5017MJD/883B	IH5052MJE/883B	IM6512MJN/883B
ICL8020MJD/883B	IH5018MJD/883B	IH5053MJE/883B	IM65X08AMFE/883B
ICL8021MTY/883B	IH5019MJE/883B	IH5108MJE/883B	IM65X08AMJE/883B
ICL8022MFD/883B	IH5020MJE/883B	IH5140MFD/883B	IM65X08MFE/883B
ICL8022MJD/883B	IH5021MJD/883B	IH5140MJE/883B	IM65X08MJE/883B
ICL8023MJE/883B	IH5022MJD/883B	IH5141MFD/883B	IM65X18AMFN/883B
ICL8038AMJD/883B	IH5023MJE/883B	IH5141MJE/883B	IM65X18AMJN/883B
ICL8038BMJD/883B	IH5024MJE/883B	IH5141MTW/883B	IM65X18MFN/883B
ICL8049BCJE/883B	IH5025MJD/883B	IH5142MFD/883B	IM65X18MJN/883B
ICL8069ACSQ/883B	IH5026MJD/883B	IH5142MJE/883B	IM65X51AMJF/883B
ICL8069BCSQ/883B	IH5027MJE/883B	IH5142MTW/883B	IM65X51MJF/883B
ICL8069CMSQ/883B	IH5028MJE/883B	IH5143MFD/883B	IM65X61AMFN/883B
ICL8069DMSQ/883B	IH5029MJD/883B	IH5143MJE/883B	IM65X61AMJN/883B
ICL8211MTY/883B	IH5030MJD/883B	IH5144MFD/883B	IM65X61MFN/883B
ICL8212MTY/883B	IH5031MJE/883B	IH5144MJE/883B	IM65X61MJN/883B
	IH188MTW/883B	IH5144MTW/883B	IM6653AMJG/883B
ICM7555MTV/883B	IH190MFD/883B	IH5145MFD/883B	IM6653MJG/883B
ICM7556MJD/883B	IH190MJE/883B	IH5145MJE/883B	IM6654AMJG/883B
	IH191MFD/883B	IH5148MFD/883B	IM6654MJG/883B
IH181MFD/883B	IH191MJE/883B	IH5148MJE/883B	
IH181MJD/883B	IH200AA/883B	IH5148MTW/883B	LM100H/883B
IH181MTW/883B	IH5032MJE/883B	IH5149MFD/883B	LM101AF/883B
IH182MFD/883B	IH5033MJD/883B	IH5149MJE/883B	LM101AH/883B
IH182MJD/883B	IH5034MJD/883B	IH5150MFD/883B	LM101H/883B
IH182MTW/883B	IH5035MJE/883B	IH5150MJE/883B	LM105H/883B
IH184MFD/883B	IH5036MJE/883B	IH5150MTW/883B	LM107F/883B
IH184MJE/883B	IH5037MJD/883B	IH5151MFD/883B	LM107H/883B
IH185MFD/883B	IH5038MJD/883B	IH5151MJE/883B	LM107J-14/883B
IH185MJE/883B	IH5040MFD/883B	IH5200MFD/883B	LM108AH/883B
IH187MFD/883B	IH5040MJE/883B	IH5200MJD/883B	LM108AJ/883B
IH187MJD/883B	IH5041MFD/883B	IH5200MTW/883B	LM108H/883B
IH187MTW/883B	IH5041MJE/883B	IH5201MJE/883B	LM110F/883B
IH188MFD/883B	IH5041MTW/883B	IH5208MJE/883B	LM110H/883B
IH188MJD/883B	IH5042MFD/883B	IH6108MJE/883B	LM111H/883B
IH200AK/883B	IH5042MJE/883B	IH6116MJI/883B	LM111J/883B
IH200AL/883B	IH5042MTW/883B	IH6201MJE/883B	LM4250H/883B
IH200MJE/883B	IH5043MFD/883B	IH6208MJE/883B	
IH201MJE/883B	IH5043MJE/883B	IH6216MJI/883B	OP-05AJ/883B
IH202MJE/883B	IH5044MFD/883B		OP-05AY/883B
IH5003MFD/883B	IH5044MJE/883B	IM5603AMFE/883B	OP-05AZ/883B
IH5003MJD/883B	IH5044MTW/883B	IM5624MFE/883B	OP-05J/883B
IH5004MFD/883B	IH5045MFD/883B	IM6100-1MJL/883B	OP-05Y/883B
IH5004MJD/883B	IH5045MJE/883B	IM6100AMJL/883B	OP-05Z/883B
IH5005MFD/883B	IH5046MFD/883B	IM6101-1MJL/883B	OP-07AJ/883B
IH5005MJD/883B	IH5046MJE/883B	IM6101AMJL/883B	OP-07AY/883B
IH5006MFD/883B	IH5047MFD/883B	IM6102-1MJL/883B	OP-07AZ/883B
IH5006MJD/883B	IH5047MJE/883B	IM6102AMJL/883B	OP-07J/883B
IH5007MFD/883B	IH5048MFD/883B	IM6103-1MJL/883B	OP-07Y/883B
IH5007MJD/883B	IH5048MJE/883B	IM6103AMJL/883B	OP-07Z/883B

APPLICATION NOTE SUMMARY

The following are brief descriptions of current Intersil Application notes.

A003 **UNDERSTANDING AND APPLYING THE ANALOG SWITCH**

Introduces analog switches and compares them to relays. Describes CMOS, hybrid (FET + driver), J-FET "virtual ground" and J-FET "positive signal" types. Application information included.

A004 **IH5009 LOW COST ANALOG SWITCH SERIES**

Compares the members of the IH5009 "virtual ground" analog switches and provides suggested applications.

A005 **THE 8007—A HIGH PERFORMANCE FET INPUT OP AMP**

Compares the 8007 with the 741, which is pin compatible and suggests applications such as log-antilog amplifier, sample and hold circuit, photometer, peak detector, etc.

A007 **USING THE 8048/8049 MONOLITHIC LOG-ANTILOG AMPLIFIER**

Describes in detail the operation of the 8048 logarithmetic amplifier, and its counterpart, the 8049 antilog amp.

A011 **A PRECISION FOUR QUADRANT MULTIPLIER—THE 8013**

Describes, in detail, the operation of the 8013 analog multiplier. Included are multiplication, division, and square root applications.

A013 **EVERYTHING YOU ALWAYS WANTED TO KNOW ABOUT THE 8038**

This note includes 17 of the most asked questions regarding the use of the 8038.

A015 **DESIGN FOR A BATTERY OPERATED FREQUENCY COUNTER**

Describes a low cost battery operated frequency/period counter using the 7207A and 7208. Includes specifications, schematics, PC layout, etc.

A016 **SELECTING A/D CONVERTERS**

Describes the differences between integrating converters and successive approximation converters. Includes a checklist for decision making, and a note on multiplexed data systems.

A017 **THE INTEGRATING A/D CONVERTER**

Provides an explanation of integrating A/D converters, together with a detailed error analysis.

A018 **DO'S AND DONT'S OF APPLYING A/D CONVERTERS**

An analysis of proper design techniques using D/A converters.

A019 **4½ DIGIT PANEL METER DEMONSTRATION/INSTRUMENTATION BOARDS**

Describes two typical PC board layouts using the 8052A/7103A 4½ digit A/D pair. Includes schematics, parts layout, list of materials, etc. Also see A028.

A020 **A COOKBOOK APPROACH TO HIGH SPEED DATA ACQUISITION AND MICROPROCESSOR INTERFACING**

Uses the building block approach to design a complete 12 volt system. Explains the significance of each component and demonstrates methods for microprocessor interfacing, including the use of control signals.

A021 **POWER D/A CONVERTERS USING THE ICH 8510**

Detailed analysis of the 8510. Included are a section describing the linearity of the device and application notes for driving servo motors, linear and rotary actuators, etc. Also see A026.

A022 **A NEW J-FET STRUCTURE—THE VARAFET**

Describes in detail the operation of the varafet, a standard J-FET with the analog gate interfacing components monolithically built-in.

A023 **LOW COST DIGITAL PANEL METER DESIGNS**

Provides a detailed explanation of the 7106 and 7107 3½ digit panel meter IC's, and describes two of the evaluation kits available from Intersil.

A026 **DC SERVO MOTOR SYSTEMS USING THE ICH8510**

This companion note to A021 explains the design techniques utilized in using the ICH8510 family to drive closed loop servo motor systems.

A027 **POWER SUPPLY DESIGN USING THE ICL8211 AND ICL8212**

Explains the operation of the ICL8211/12 and describes various power supply configurations. Included are positive and negative voltage regulators, constant current source, programmable current source, current limiting, voltage crowbarring, power supply window detector, etc.

A028 **BUILDING AN AUTO RANGING DMM WITH THE ICL7103A/8052A CONVERTER PAIR**
This companion app note to A019 explains the use of the 8052A/7103A converter pair to build a ±4½ digit auto ranging digital multimeter. Included are schematics, circuit descriptions, tips and hints, etc.

A029 **POWER OP AMP HEAT SINK KIT**
Describes the heat sinks for the ICH8510 family. These heat sinks may be ordered from the factory.

A030 **THE ICL7104: A BINARY OUTPUT A/D CONVERTER FOR MICROPROCESSORS**
Describes in detail the operation of the 7104. Includes in digital interfacing, handshake mode, buffer gain, auto-zero and external zero. Appendix includes detailed discussion of auto-zero loop residual errors in dual slope A/D conversion.

A031 **COIL DRIVE ALARM DESIGN CONSIDERATIONS**
Explains the procedure used when using watch circuits to drive piezoelectric transducers.

A032 **UNDERSTANDING THE AUTO-ZERO AND COMMON MODE PERFORMANCE OF THE ICL7106/7107/7109 FAMILY**
Explains in detail the operation of the ICL7106/7/9 family of A/D Converters.

A046 **BUILDING A BATTERY OPERATED AUTO RANGING DVM WITH THE ICL7106**
Explains principles of auto ranging, problems and solutions. Includes clock circuits, power supply requirements, design hints, schematics, etc.

A047 **GAMES PEOPLE PLAY WITH A/D CONVERTERS**
Describes 25 different integrating A/D converter applications. Input circuits, conversion modifications, display and microprocessor interfaces are shown in detail.

A050 **USING THE IT500 FAMILY TO IMPROVE THE INPUT BIAS CURRENT OF BIFET OP AMPS**
A brief description of a preamplifier for BIFET OP AMPS.

A051 **PRINCIPLES AND APPLICATIONS OF THE ICL7660 CMOS VOLTAGE CONVERTER**
Describes internal operation of the ICL7660. Includes a wide range of possible applications.

A052 **TIPS FOR USING SINGLE CHIP 3½ DIGIT A/D CONVERTERS**
Answers frequently asked questions regarding the operation of 3½ digit single chip A/D converters. Included are sections on power supplies, displays, timing and component selection.

A053 **THE ICL7650 A NEW ERA IN GLITCH-FREE CHOPPER STABILIZER AMPLIFIERS**
A brief discussion of the internal operation of the ICL7650, followed by an extensive applications section including amplifiers, comparators, log-amps, pre-amps, etc.

A054 **DISPLAY DRIVER FAMILY COMBINES CONVENIENCE OF USE WITH MICROPROCESSOR INTERFACABILITY**
Compares and describes the various display drivers. Includes design examples for 7 segment, Alpha-numeric, and bargraph systems.

M011 **AVOIDING PROBLEMS IN CMOS MEMORY OPERATION**
Discusses input overvoltage and SCR latch-up and the multiple address access problem in CMOS RAMs.

EVALUATION KITS AVAILABLE FROM INTERSIL

PRODUCT DESCRIPTION	PART NUMBER	CONTENTS
3½ Digit LCD Panel Meter Kit	ICL7106EV/KIT	ICL7106 + PC Card + All Passive Components
3½ Digit LED Panel Meter Kit	ICL7107EV/KIT	ICL7107 + PC Card + All Passive Components
3½ Digit Low Power LCD Panel Meter Kit	ICL7136EV/KIT	ICL7136 + PC Card + All Passive Components
4½ Digit A/D Converter Kit	ICL7135EV/KIT	ICL7135 + ICL7660 + ICL8069 + PC Card + Active, Passive Components
4½ Digit LCD Display Driver Kit	ICM7211EV/KIT	ICM7211 + 4½ Digit LCD Display + PC Card + Active, Passive Components
4½ Digit LED Display Driver Kit	ICM7212EV/KIT	ICM7212 + 4½ Digit LED Display + PC Card + Active, Passive Components
4½ Digit VF Display Driver Kit	ICM7235EV/KIT	ICM7235 + 4½ Digit VF Display + PC Card + Active, Passive Components
8 Character Multiplexed LCD Display Driver Kit	ICM7233 EV/KIT	2 of ICM7233 + PC Card + 8 Character Triplexed LCD Display
8 Character Multiplexed LED Display Driver Kit	ICM7243BEV/KIT	ICM7243B + PC Card + 8 Character LED
4½ Digit LCD Display Counter Kit	ICL7224EV/KIT	ICM7224 + ICM7207A + 5.24288 MHz Crystal + 4½ Digit LCD Display + PC Card + Passive Components
4½ Digit LED Display Counter Kit	ICM7225EV/KIT	ICM7225 + ICM7207A + 5.24288 MHz Crystal + 4½ Digit LED Display + PC Card + Passive Components
4½ Digit VF Display Counter Kit	ICM7236EV/KIT	ICM7236 + ICM7207A + 5.24288 MHz Crystal + 4½ Digit VF Display + PC Card + Passive Components
8 Digit Stopwatches		
Hour Decade Timer	ICM7045AEV/KIT H	ICM7045A + 3.640889 MHz Crystal
Minute Decade Timer	ICM7045AEV/KIT M	ICM7045A + 2.184533 MHz Crystal
4 Function/24 Hour Clock	ICM7045EV/KIT	ICM7045 + 6.5536 MHz Crystal
6 Digit Stopwatches		
4 Function	ICM7215EV/KIT	ICM7215 + 3.2768 MHz Crystal
Touch Tone Encoder		
One contact per key	ICM7206EV/KIT	ICM7206 + 3.579545 MHz Crystal
Two contacts per key, common to positive supply	ICM7206AEV/KIT	ICM7206A + 3.579545 MHz Crystal
Common to negative supply, oscillator enabled when key depressed	ICM7206BEV/KIT	ICM7206B + 3.579545 MHz Crystal
8 Digit Frequency/Period Counter		
5 Function	ICM7226AEV/KIT	ICM7226A + 10 MHz Crystal + PC Card + LEDs + All Passive Components
Oscillator Controller		
For application as freq. counter with ICM7208	ICM7207EV/KIT	ICM7207 + 6.5536 MHz Crystal
	ICM7207AEV/KIT	ICM7207A + 5.24288 MHz Crystal
Power Amplifier Kits	ICH8510IEV/KIT	ICH8510I + Socket + Heat Sink
	ICH8510MEV/KIT	ICH8510M + Socket + Heat Sink
	ICH8520IEV/KIT	ICH8520I + Socket + Heat Sink
	ICH8520MEV/KIT	ICH8520M + Socket + Heat Sink
	ICH8530IEV/KIT	ICH8530I + Socket + Heat Sink
	ICH8530MEV/KIT	ICH8530M + Socket + Heat Sink

FET, MOSFET, AND DUAL TRANSISTOR CHIPS

INTRODUCTION

Intersil recognizes the increasing need for transistors and FETs in die form. To fulfill this need, Intersil offers a full line of JFETs, MOSFETs, and dual transistors in die form.

Die sales do, however, present some unique problems. In many cases the chips cannot be guaranteed to the same electrical specifications as the packaged part. This is due to the fact that leakage, noise, AC parameters and temperature testing cannot be tested to the same degree of accuracy for dice as it can for packaged devices. This is due to equipment limitations and handling problems.

PURCHASE OPTIONS

Intersil offers dice which are delivered in a number of forms:

- Chips which have been electrically probed, inked, visually inspected and diced.
- Wafers which have been electrically probed, inked, visually inspected and scribed only.
- Wafers which have been electrically probed, inked, and visually inspected only.

GENERAL PHYSICAL INFORMATION

- Consult individual product information sheets for dimensions. Except for the aluminum bonding pads, the chips are completely covered with vapox (silicon dioxide). This minimizes damage to the chip caused by handling problems.
- Dice are 100% tested to electrical specifications, then visually inspected. When wafers are ordered, dice which fail the electrical test are inked out.
- Generally the minimum size of the die-attaching pad metallization should be at least 5 mils larger (on every edge) than the chip dimensions. For example, a 15 mil chip should be attached on at least a 25 mil pad.

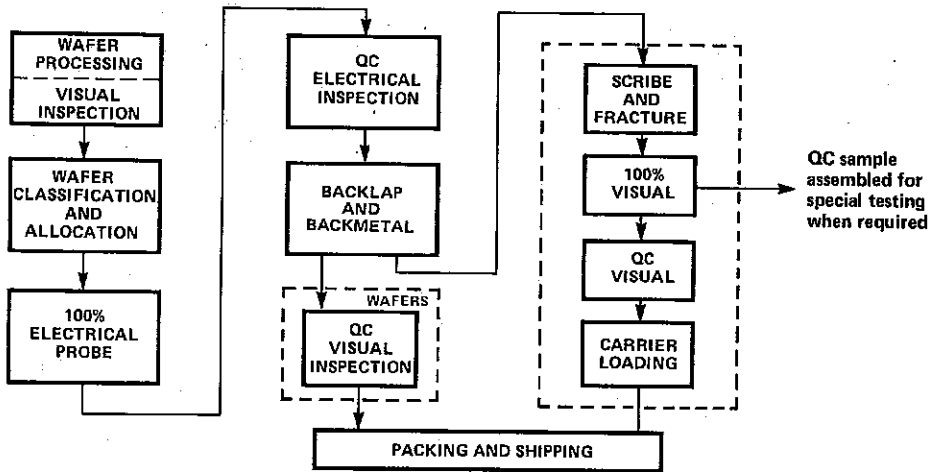
Small Signal Devices

- Chips are available with exact length X width dimensions plus tolerance (see individual data sheets). Chip height ranges from .003" to .006".
- To facilitate die attaching, chips are gold backed. Approximate thickness is 1000 angstroms. In general, dice should be attached to gold, platinum, or palladium metallization. Thin-film gold, moly-gold and most of the thick-film metallization materials are compatible.
- All chips have aluminum metallization and aluminum bonding pads. Typical aluminum thickness is 12,000 angstroms.

Power FETs

- Chip height ranges from .007" to .020".
- To facilitate die attaching, chips have gold or silver backing.
- Top side metal is aluminum with a thickness of 10,000 - 30,000 angstroms.

CHIP AND WAFER PROCESSING FLOW CHART



B

RECOMMENDED DICE ASSEMBLY PROCEDURE

CLEANING

Dice supplied in die form do not require cleaning prior to assembly. Dice supplied in wafer form should be cleaned after scribing and breaking. Freon TF in a vapor degreaser is the preferred cleaning method. However, an alternative is to boil the die in TCE for five minutes with a rinse in isopropyl alcohol for 1-2 minutes.

DIE ATTACH:

The die attach operation should be done under a gaseous nitrogen ambient atmosphere to prevent oxidation. A preform should be used if the mounting surface has less than 50 microinches of gold and the die should be handled on the edges with tweezers. Die attach temperature should be between 385° C and 400° C with eutectic visible on three sides of the die after attachment.

BONDING:

Thermocompression gold ball or aluminum ultrasonic bonding may be used. The gold ball should be about 3 times the diameter of the gold wire. The ball should cover the bonding pad, but not excessively, or it may short out surrounding metallization. 1-mil aluminum wire may be used on most dice, but should not be used if the assembled unit will be plastic encapsulated.

HANDLING OF DICE:

All dice shown in this catalog are passivated devices and Intersil warrants that they will meet or exceed published specifications when handled with the following precautions:

- Dice should be stored in a dry inert-gas atmosphere.
- Dice should be assembled using normal semiconductor techniques.
- Dice should be attached in a gaseous nitrogen spray at a temperature less than 430° C.

ELECTRICAL TEST LIMITATIONS

B

DUAL BIPOLAR TRANSISTORS

LV_{CEO}	100V max. @ ≤1 mA
BV_{CBO}	100V max. @ ≥1 μA
BV_{EBO}	100V max. @ ≤10 mA
h_{FE}	≤1000 @ ≥10 μA
$V_{CE(sat)}$	≥10 mV @ ≤10 mA
I_{CBO}	≥100 pA @ ≤100V
$V_{BE1}-V_{BE2}$	≥1 mV @ ≥10 μA
$I_{B1}-I_{B2}$	≥2 nA

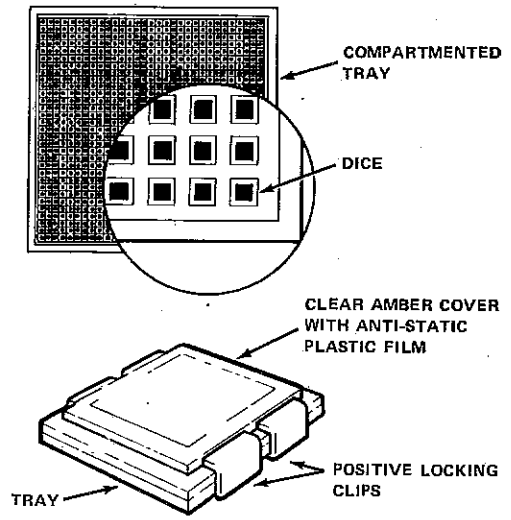
FETS

Breakdown voltage	100V max. @ 1 μA
Pinch-off voltage	0-20V @ ≥1 nA
$V_{GS(th)}$	0-20V @ ≥10 μA
$r_{DS(on)}$	20 Ω min. @ V_{GS} = 0 (V_{GS} = 30 MOSFETs)
I_{DSS} & I_{DSS}	100 mA max.
g_{fs}	10,000 μMHOS max. @ I_D ≤ 10 mA
$I_{D(off)}$, $I_{S(off)}$, I_{GSS}	100 pA min.
$V_{GS1} - V_{GS2}$ (Duals)	10 mV min.

Electrical testing is guaranteed to a 10% LTPD. AC parameters such as capacitance and switching time cannot be tested in wafer or dice form.

STANDARD DIE CARRIER PACKAGE

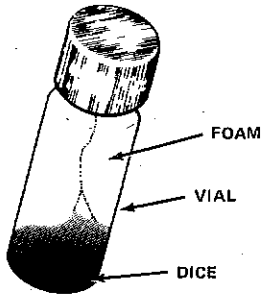
- Easy to handle, store and inventory.
- 100% electrically probed dice with electrical rejects removed.
- 100% visually sorted with mechanical and visual rejects removed.
- Easy visual inspection — dice in carriers, geometry side up.
- Individual compartment for each die.
- Carriers usuable in customer production area.
- Carrier may be storage container for unused dice.
- Carriers hold 25, 100, or 400 dice, depending on die size and quantity ordered.
- Part numbers shown in this catalog are for carrier packaging.



DIE & WAFER ORDERING INFORMATION

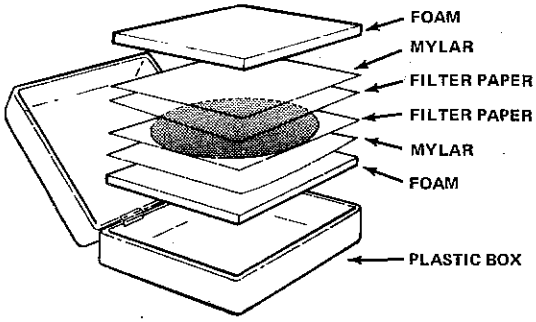
OPTIONAL VIAL PACKAGE

- 100% electrically probed dice with rejects inked but included in vial. Bulk shipment.
- 10% extra good dice included (no charge) to cover possible breakage and/or visual rejects.
- Preferred for production quantities.
- Lower cost.
- For vial package – replace "D" in catalog number with "V", e.g.: 2N4416/D (2N4416 dice in carrier) becomes 2N4416/V (2N4416 dice in vial).



OPTIONAL WAFER PACKAGE

- 100% electrically probed – rejects inked.
- 10% extra good dice included (no charge) to cover possible breakage and/or visual rejects.
- Preferred for production quantities.
- Lowest cost.
- Wafer is supplied unscribed.
- For wafer package – replace "D" in catalog number with "W", e.g.: 2N4416/D (2N4416 dice in carrier) becomes 2N4416/W (2N4416 dice in wafer).



NOTE:

Intersil reserves the right to improve device geometries and manufacturing processes as required. These improvements may result in slight geometry changes. However, they will not affect the electrical limits, basic pad layouts or maximum die sizes in this catalog.

ELECTRICAL TEST CAPABILITY

As an example of how to use the capability chart to see what Intersil actually guarantees and tests for, on a 100% basis, compare the 2N4391 in a TO-18 package to the 2N4391 delivered as a chip.

Electrical Test Spec.	2N4391 in a TO-18	2N4391 Chip
I_{GSS} @ 25C	100 pA max.	100 pA max.
BV_{GSS}	40V min.	40V min.
$I_{D(off)}$ @ 25C	100 pA max.	100 pA max.
$V_{GS(forward)}$	1V max.	See note 1
$V_{GS(off)}$ or V_P	4V to 10V	4V to 10V
I_{DSS}	50 to 150 mA	50 to 100 mA
$V_{DS(on)}$	0.4V max.	0.4V max.
$r_{DS(on)}$	30Ω max.	30Ω max.
C_{iss}	14 pF max.	Guaranteed by Design
C_{rss}	3.5 pF max.	Guaranteed by Design
t_d	15ns max.	Guaranteed by Design
t_r	5ns max.	Guaranteed by Design
t_{off}	20ns max.	Guaranteed by Design
t_f	15 ns max.	Guaranteed by Design

NOTE 1: This parameter is very dependent upon quality of metallization surface to which chip is attached.

SUMMARY

Of the 14 items specified for the package part, only 7 can be tested and guaranteed in die form. It is to be noted that those specifications which cannot be tested in die form can be sample tested in package form as an indicator of lot performance. Many of the tests, however, such as capacitance tests, are design parameters.

The above electrical testing is guaranteed to a 10% LTPD. However, there are occasions where customer requirements cannot be satisfied by wafer sort testing alone. While the previously described tests will be done on a 100% basis, Intersil recognizes the need for additional testing to obtain confidence that a particular customer's needs can be met with a reasonably high yield. Toward this end Intersil has instituted a dice sampling plan which is two-fold. First, random samples of the dice are packaged and tested to assure adherence to the electrical specification. When required, wafers are identified and wafer identity is tied to the samples. This tests both the electrical character of the die and its ability to perform electrically after going through the high temperature dice attachment stage. Second, more severe testing can be performed on the packaged devices per individual customer needs. When testing is required other than that called out in the data sheet, Intersil issues an ITS number to describe the part. Examples of tighter testing which can be performed on packaged samples is shown as follows:

DIE & WAFER ORDERING INFORMATION

FET & DUAL FET PAIRS

1. Leakages to 1 pA (I_{GSS})
2. $r_{DS\ (on)}$ to as low as 4 ohms
3. $I_{D\ (off)}$ to 10 pA
4. I_{DSS} to 1 amp (pulsed)
5. g_{fs} to 10,000 μmho
6. g_{os} to 1 μmho
7. e_n noise to 5 nV/$\sqrt{Hz}$ at frequencies of 10 Hz to 100 Hz
8. CMRR to 100 dB
9. $\Delta(V_{GS1}-V_{GS2})/\Delta T$ down to 10μV/°C to an LTPD of 20%
10. g_m match to 5%
11. I_{DSS} match to 5%

TRANSISTOR PAIRS

1. Leakages to as low as 1 pA
2. Beta with collector current up to 50 mA and as low as 100 nA
3. f_T up to 500 MHz with collector currents in the range of 10 μA to 10 mA
4. Noise measurements as low as 5 nV/$\sqrt{Hz}$ from 10 Hz to 100 kHz
5. $\Delta(V_{BE1}-V_{BE2})/\Delta T$ to 10μV/°C to an LTPD of 20%

VISUAL INSPECTION

Individual chips are 100% inspected to MIL-STD-750, Method 2072 or, as an option, MIL-STD-883, Level B. Inspection is done to an LTPD of 20%. As an option, Intersil offers S.E.M. capability on all wafers.

CMOS INTEGRATED CIRCUIT CHIPS

INTRODUCTION

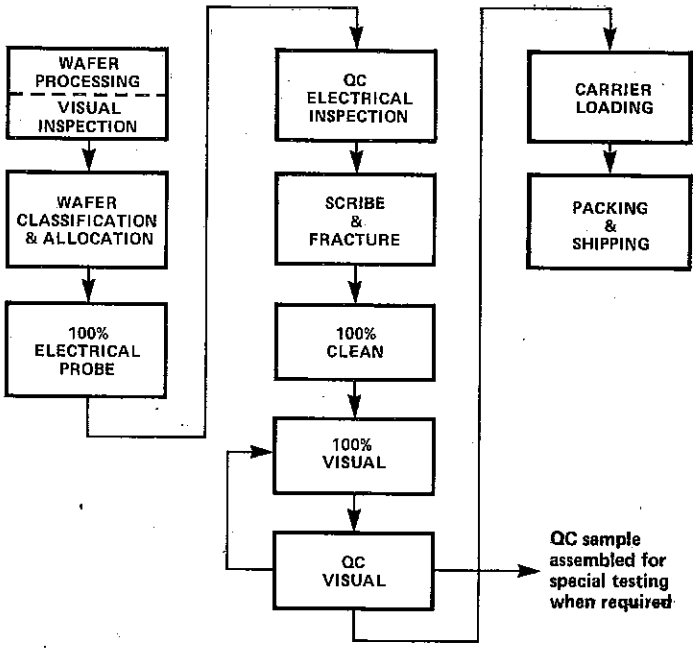
In addition to discrete device chips, Intersil also offers a full line of metal gate CMOS integrated circuits in die form. Die sales, however, present some unique problems. In many cases, chips cannot be guaranteed to the same electrical specifications as can the packaged parts. This is because leakage, noise, AC parameters and temperature testing cannot be guaranteed to the same degree of accuracy for dice as for packaged devices.

GENERAL PHYSICAL INFORMATION

- Chips are available with precise length and width dimensions, ±2 mils in either dimension.
- Chip thickness is 15 mils ±1 mil.
- Bonding pad and interconnect material is aluminum, 10K to 15K Å thick.
- Each die surface is protected by planar passivation and additional surface glassivation except for bonding pads and scribe lines. The surface passivation is removed from the bonding pad areas by an HF etchant; bonding pads may appear discolored at low magnification due to surface roughness of the aluminum caused by the etchant.
- Dice are 100% inspected to electrical specifications, then visually inspected according to MIL-STD-883, Method 2010.2, Condition B, with modifications reflecting CMOS requirements.
- Bonding pad dimensions are 4.0 x 4.0 mils minimum.
- Storage temperature is -40°C to +150°C.
- Operating temperature is -20°C to +70°C.
- Guaranteed AQL Levels:

Visual	2.0%
Functional electrical testing	1.0%
Parametric DC testing	4.0%
Untested parameters	10.0%

CMOS INTEGRATED CIRCUIT CHIP PROCESSING FLOW CHART



B

RECOMMENDED DICE ASSEMBLY PROCEDURES

CLEANING

Dice supplied in die form do not require cleaning prior to assembly. However, if cleaning is desired, dice should be subjected to freon TF in a vapor degreaser and then vapor-dried.

RECOMMENDED HANDLING

Intersil recommends that dice be stored in the vacuum-sealed plastic bags which hold the dice carriers. Once removed from the sealed bags, the dice should be stored in a dry, inert-gas atmosphere.

Extreme care should be used when handling dice. Both electrical and visual damage can occur as the result of an unclean environment or harsh handling techniques.

DIE ATTACH

The die attach operation should be done under a gaseous nitrogen ambient atmosphere to prevent oxidization. If a eutectic die attach is used, it is recommended that a 98% gold/2% silicon preform be used at a die attach temperature between 385°C and 435°C. If an epoxy die attach is used, the epoxy cure temperature should not exceed 150°C. If hermetic packages are used, epoxy die attach should be carried out with caution so that there will be no "outgassing" of the epoxy.

BONDING

Thermocompression gold ball or aluminum ultrasonic bonding may be used. The wire should be 99.99% pure gold and the aluminum wire should be 99% aluminum/1% silicon. In either case, it is recommended that 1.0 mil wire be used for normal power circuits.

STANDARD DIE CARRIER PACKAGE

- Easy to handle, store and inventory.
- 100% electrically probed with electrical rejects removed.
- 100% visually sorted with mechanical and visual rejects removed.
- Easy visual inspection — dice are in carriers, geometry side up.
- Individual compartment for each die.
- Carriers usable in customer production area.
- Carrier may be used as storage contained for unused dice.
- Carriers hold 25, 100 or 400 dice, depending on die size and quantity ordered.
- Packaging of integrated circuit dice in carriers is identical to illustration shown earlier for discrete device, except that IC chips are not available in vial packs or in wafer form.

CHANGES

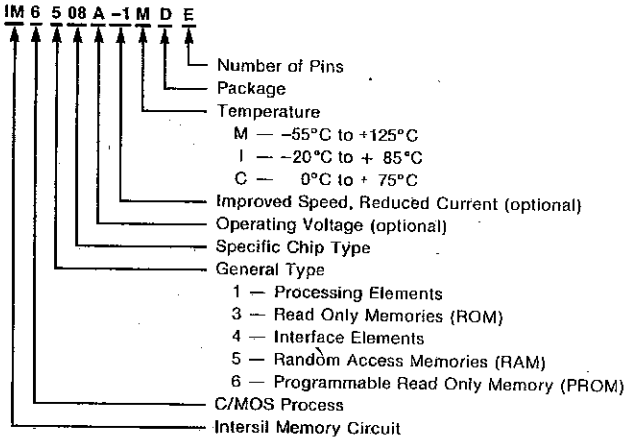
Intersil reserves the right in improve device geometries and manufacturing processes without prior notice. Although these improvements may result in slight geometry changes, they will not affect dice electrical limits, pad layouts, or maximum die sizes.

USER RESPONSIBILITY

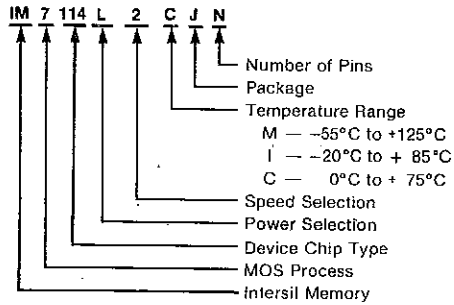
Written notification of any non-conformance by Intersil of Intersil's dice specifications must be made within 75 days of the shipment date of the die to the user. Intersil assumes no responsibility for the dice after 75 days or after further user processing such as, but not limited to, chip mounting or wire bonding.

PART NUMBERS AND ORDERING INFORMATION

C/MOS MEMORY:



MOS MEMORY:



B

DIE & WAFER ORDERING INFORMATION

FET & DUAL FET PAIRS

1. Leakages to 1 pA (I_{GSS})
2. $r_{DS\ (on)}$ to as low as 4 ohms
3. $I_{D\ (off)}$ to 10 pA
4. I_{DSS} to 1 amp (pulsed)
5. g_{fs} to 10,000 μmho
6. g_{os} to 1 μmho
7. e_n noise to 5 nV/$\sqrt{Hz}$ at frequencies of 10 Hz to 100 Hz
8. CMRR to 100 dB
9. $\Delta(V_{GS1}-V_{GS2})/\Delta T$ down to 10μV/°C to an LTPD of 20%
10. g_m match to 5%
11. I_{DSS} match to 5%

TRANSISTOR PAIRS

1. Leakages to as low as 1 pA
2. Beta with collector current up to 50 mA and as low as 100 nA
3. f_T up to 500 MHz with collector currents in the range of 10 μA to 10 mA
4. Noise measurements as low as 5 nV/$\sqrt{Hz}$ from 10 Hz to 100 kHz
5. $\Delta(V_{BE1}-V_{BE2})/\Delta T$ to 10μV/°C to an LTPD of 20%

VISUAL INSPECTION

Individual chips are 100% inspected to MIL-STD-750, Method 2072 or, as an option, MIL-STD-883, Level B. Inspection is done to an LTPD of 20%. As an option, Intersil offers S.E.M. capability on all wafers.

PART NUMBERING SYSTEM

Examples of Intersil Part Numbers

BASIC	ELECTRICAL OPTION	TEMP	PKG	PIN	ORDER #
ICH8500	A	C	T	V	ICH8500ACTV
ICL8038	C	C	P	D	ICL8038CCPD
IH5040		M	D	E	IH5040MDE

ON ALL INTERSIL IC PART NUMBERS. THE LAST THREE LETTERS ARE TEMPERATURE, PACKAGE, AND NUMBER OF PINS, RESPECTIVELY.

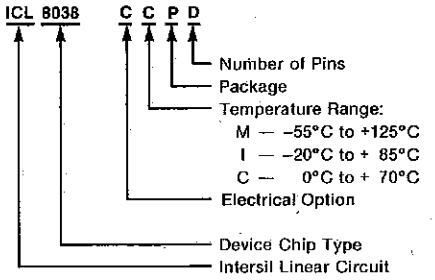
PACKAGE:

A	TO-237
B	Plastic flat-pack
C	TO-220
D	Ceramic dual-in-line
E	Small TO-8
F	Ceramic flat-pack
H	TO-66
I	16 pin (.6 x .7 pin spacing) hermetic hybrid dip
J	Cerdip dual-in-line
K	TO-3
L	Leadless, ceramic
P	Plastic dual-in-line
S	TO-52
T	TO-5 type (also TO-78, TO-99, TO-100)
U	TO-72 type (also TO-18, TO-71)
V	TO-39
Z	TO-92
/W	Wafer
/D	Dice

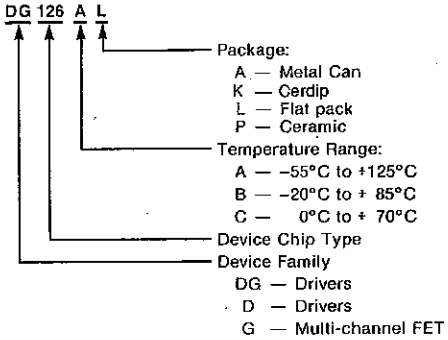
NUMBER OF PINS:

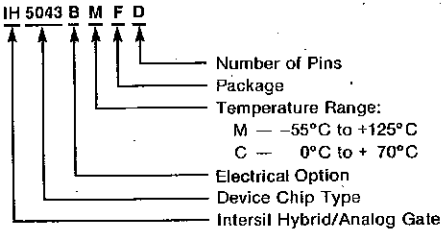
A	8	P	20
B	10	Q	2
C	12	R	3
D	14	S	4
E	16	T	6
F	22	U	7
G	24	V	8 (0.200" pin circle, isolated case)
H	42		
I	28	W	10 (0.230" pin circle, isolated case)
J	32		
K	35	Y	8 (0.200" pin circle, case to pin 4)
L	40		
M	48	Z	10 (0.230" pin circle, case to pin 5)
N	18		

LINEAR:

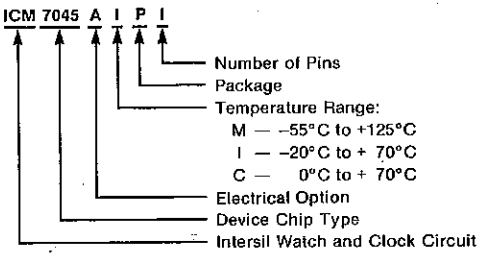


HYBRIDS:





WATCH AND CLOCK:



B